New Concepts For The Production Of HDI Printed Circuit Boards

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Abstract

The demands for the production of HDI printed circuits can be compared and contrasted for hand held devices and for IC substrate technology however in both these application areas the demands are changing rapidly driven by the need to increase interconnect density.

In the case of hand held devices typically the production of track line and space of 100 µm is moving to currently 75 µm with future target of 50µm, for IC substrate the current demand is in the region of 28 µm line and space but this is being pushed rapidly towards 20 µm.

This paper presents developments in copper plating process and equipment to ensure best possible quality and production yield in HDI production for both application areas.

The use of insoluble anodes is presented as one of the main factors in the improvement in production quality together with the associated copper plating electrolyte. The advantages and disadvantages in panel and also pattern plating systems are presented and discussed together with combined solutions for blind micro via copper filling and also through via copper filling.

Introduction

The changing requirements for line and space capability place great demands on the copper plating process used to produce the conductive tracks on printed circuit boards. The plating process itself is only one step in the production sequence and other areas are also critical in achieving the required tolerances for example the imaging step before copper plating or the further processing of the panels after copper plating through etching or resist stripping processes. Nevertheless the copper plating process must be optimised to achieve process security and subsequent yields in the entire production process and also to enable best results in the other processing steps.

Traditionally the copper plating of printed circuit boards has been with either a “panel” or a “pattern” plate technique, for production of HDI printed circuit boards both of these techniques have advantages and disadvantages.

The advantages of the panel plate process are as follows,

- Plated copper distribution on the panel surface and in the hole dependant on equipment set up and generally easy to optimise.
- No over-plating of dry film resist possible.
- Etching parameters after copper plating can be adjusted to meet the copper thickness over the whole panel.
- Relatively constant track cross section over the whole panel gives yield advantages when tight impedance control specifications are required.

However the panel plate process has also disadvantages,

- Resist tenting for HDI requires advanced imaging process depending on the image complexity.
- The panel plated copper must be etched together with the copper foil to produce the tracks, this can lead to undercut and poor track definition especially for HDI applications. This problem may be exaggerated by variations in the circuit pattern on the panel, large track density areas are etched slower than isolated track areas where over-etching is difficult to prevent.
- The full copper etching process has increased cost factor and also environmental impact due to the amount of copper etched.

The alternative pattern plating process can be characterized by the following advantages,

- The copper which must be etched is only the thickness of the copper foil used which greatly reduces the danger of under-etching.

On the other hand the disadvantages of the pattern plate process are,

- Significant variation of the plated copper thickness over the surface of the panel strongly dependant on the image to be plated. This leads to difficulties meeting tighter impedance control specifications.

- Danger of over-plating of the dry film image also dependant on the image complexity which can make resist stripping difficult or even impossible.
- The imaging process for HDI in pattern plate also requires an advanced imaging process or significant variation in line and space width may be experienced.

Figure 1: *Comparison of standard copper plating methods.*

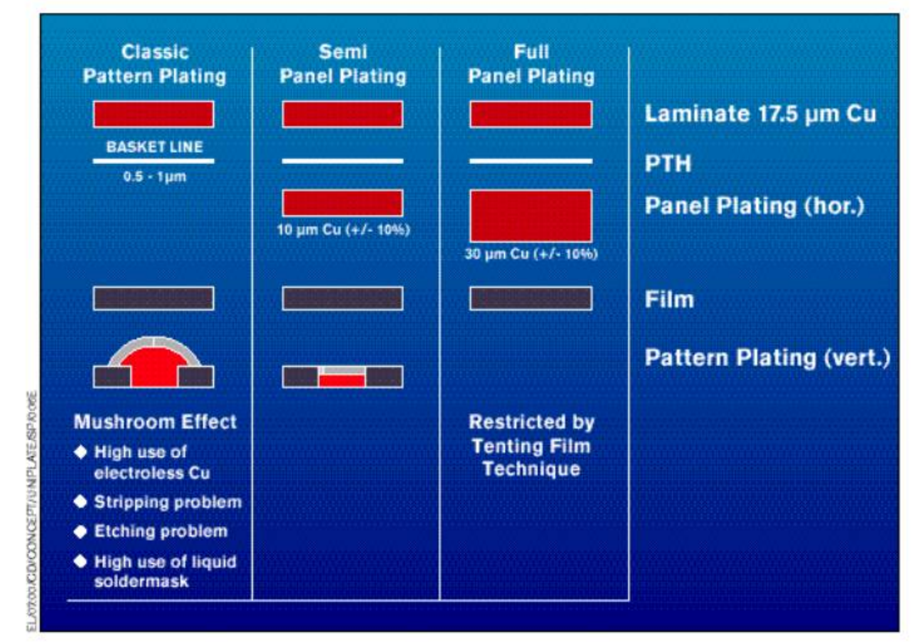
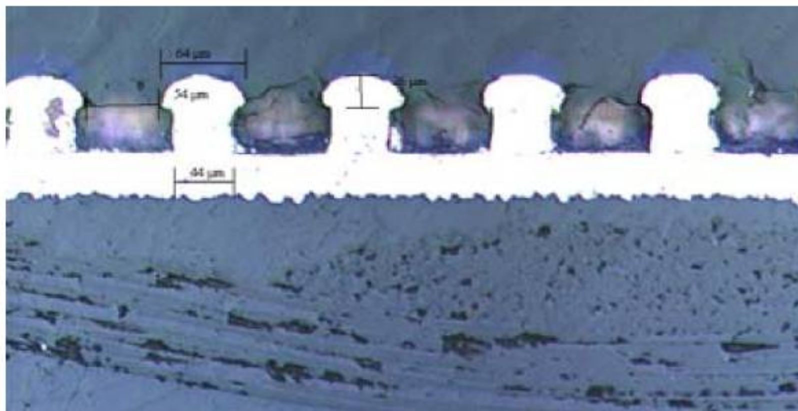


Figure 2 shows the typical result in cross section of "mushrooming" of plated copper over the photoresist with imaged track width approx. 44µm. The resist is extremely difficult to remove and will prevent subsequent copper etching.

Figure 2: *Copper over plate in pattern plating causing lock in of photo resist.*



As a compromise a combination of panel and pattern copper plating may be used which aims to combine the processing advantages,

- Lower copper required to be etched than in full panel plate.
- Panel and pattern plate copper deposit thickness may be adjusted to meet the specific product demands.
- Copper etching parameters may be more easily optimised.

However the advantages are still offset by the following,

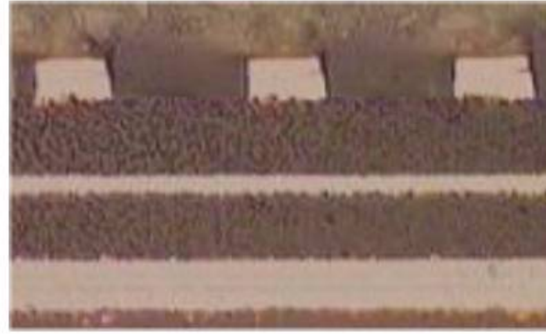
- The copper to be etched is still thicker than only the copper foil so more under-etching will be seen than in pattern plating.

- More process steps are used for the copper plating giving more potential for handling difficulties and subsequent yield loss particularly if a mixture of horizontal and vertical systems are used.

For the highest requirements in line and space for HDI production one of the most important questions is how much total copper can be etched to meet the specification. To achieve best results it is common to use thinner base material copper foil. In the latest state of the art production using panel plate methods depositing 30 µm copper approx. 70 µm line and space can be achieved using copper foil in the range 3 µm. For the case of IC substrate production this reduction in the copper foil is taken to the extreme where the copper “foil” is the approx. 0.7 – 1 µm thick electroless copper deposited over the whole of the prepared base material, this allows production of line and space in the range 25 – 30 µm as part of the semi additive process. A key feature of this semi-additive or “SAP” process is the use of flash etch of the electroless copper to finish circuitisation of the plated surface. Figure 3 shows the circuitised track area in micro-section after flash etch of an IC substrate.

Figure 3: *Pattern plating in the “SAP” process for IC substrate production.*

„SAP“ pattern plate tracks after flash etch process



The plated copper distribution, whether in panel or pattern plating mode or a combination of the two is critical in achieving the highest specification demands and enabling consistent further production. The use of insoluble anodes in the copper plating process gives consistent reproducible results with the added advantage of elimination of any production stop due to anode maintenance, these advantages have been described in [1] together with the use of an iron redox system for copper replenishment. An alternative method for copper replenishment with insoluble anode systems is with copper oxide or carbonate which is dissolved depending on throughput in a separate cell and then filtered into the working electrolyte. However there are disadvantages associated with this system as follows,

- Oxygen generation at the anodes causing high organic consumption and potential anode lifetime issues.
- Gas bubbles in the working electrolyte with possible impact on blind micro via production.
- Negative cost impact in the use of copper oxide or carbonate.

The copper oxide or carbonate used should have the highest purity to ensure plated copper quality. The most common contaminant found is chloride and this can have a very detrimental effect on the plating process as the standard chloride working range of 40 – 60 mg/l can be very quickly exceeded. The use of the iron redox system with copper metal has the advantage here as high purity copper clippings are readily available at a significantly lower price than that for copper oxide or carbonate.

Equipment characteristics for HDI production system.

In production systems extreme price pressure is driving the demand for higher productivity. One aspect of this is the price increase in raw materials particularly copper however as always a compromise between reliability, quality and economical factors must be found

These challenges for a production system for HDI printed circuit boards can be summarized as follows,

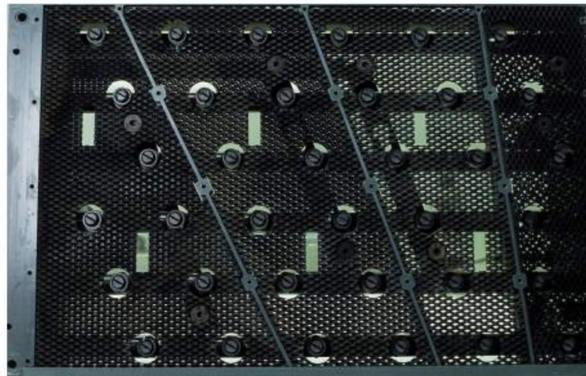
- Low surface plating thickness with best possible surface distribution.
- Capability for constant surface distribution on thin copper foil base material at high applied current densities.
- Good copper throwing power in through holes and also plated blind micro vias.
- Smallest dimple with blind micro via filling without inclusion.

- High productivity through optimum equipment efficiency including current density.
- No surface contamination or roughness or contamination of copper deposit from raw materials.
- Advanced material handling to enable production of thin cores with copper foil in the range 1 – 5µm

To meet these challenges the latest horizontal production systems are equipped with a number of special features. Insoluble anode systems are standard but the latest versions are equipped with segmented anodes and associated individually controlled rectifiers supplying the correct current to each anode segment to ensure best surface distribution with thin copper foil.
Figure 4 shows the design of the segmented anodes used in Inpulse processing systems to ensure both optimum surface distribution and also compatibility with conveyorised processing.

Figure 4: *Segmented anode for optimal surface distribution.*

Segmented anode with four independently controlled sections



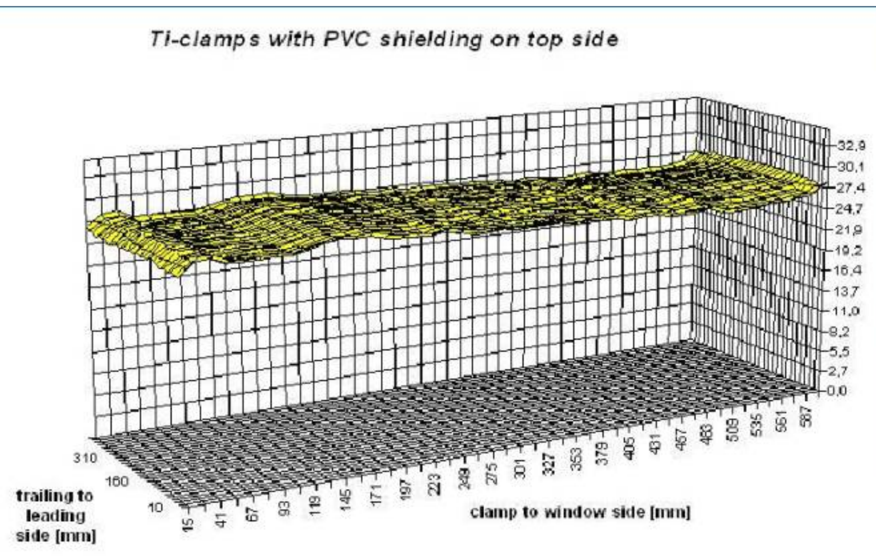
The rectification system must be capable of supplying constant DC or pulse plating with clearly defined pulse plating characteristics with provision for pause or even phase shift between anodes.
The electrical contact to the panel is critical especially with thin copper foil at high applied current densities, if the contact area is not large enough then the copper foil will be damaged or even burned away due to the increased contact resistance. A typical clamp suitable for both thin material and also thin copper foil as used in horizontal Inpulse processing equipment is shown in figure 5.

Figure 5: *High performance clamp for thin copper foil and thin panel capability.*

Clamp for thin panel process with large contact area

Figure 6 shows the surface distribution achieved on panels with copper foil in the range 3-5 µm plated at 9 A/dm² effective using the featured segmented anode systems with thin foil clamps.

Figure 6: *Surface distribution achieved on panel with 3-5 µm copper foil*



The plated copper distribution is primarily dependant on the equipment set up and as shown above optimum results of less than ± 10% can be achieved at high current densities even with thin copper foil. The measurement of the surface distribution was within 10mm from the edge of the panel except at the clamp side where measurement started 15 mm from the edge. The plating system using these features gives a ± 10% surface distribution over almost 92% of an 18" by 24" panel.

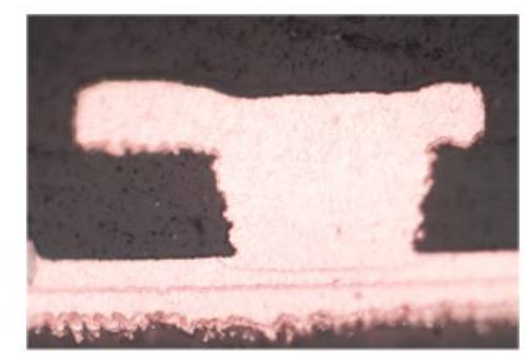
Blind micro via filling with minimum surface copper plating.

Blind micro via filling with electrolytic copper is becoming a standard requirement for HDI printed circuit boards. Filling can be achieved simply by plating enough copper on the surface of the panel however the current density must then be low enough to prevent formation of inclusions, further aspects of the theory and application of blind micro via filling have been discussed in [2].

For HDI applications the requirement is to achieve inclusion free blind micro via filling and also to enable fine line structuring, again this process can be made in either panel or pattern plating conditions.

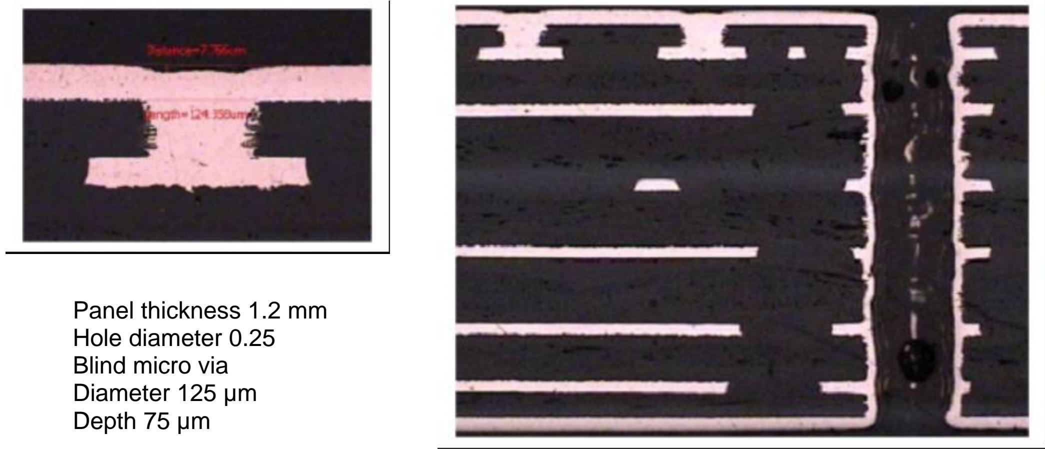
The production of IC substrate uses the pattern plate mode to achieve via filling, an example is shown in figure 7 where use of insoluble anodes in vertical equipment under DC plating conditions ensures optimum surface distribution.

Figure 7: *Blind micro via filling as pattern plate process for IC substrate*



For IC substrate production through vias are not normally present but this added factor is present in panels intended for hand held devices. Figure 8 shows a micro-section through a typical printed circuit with plated through hole as well as filled blind micro-vias. The panel was plated at 1.5 A/dm² in a vertical line equipped with insoluble anodes, the blind micro via filling quality is constant and with constant surface distribution.

Figure 8: *Printed circuit board with through holes and also filled blind micro vias*

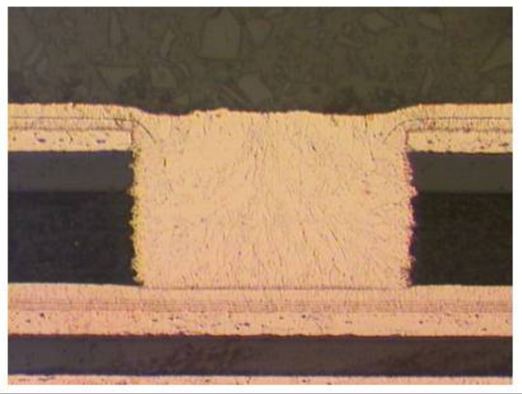


Panel thickness 1.2 mm
Hole diameter 0.25
Blind micro via
Diameter 125 µm
Depth 75 µm

In horizontal panel plating the use of selected electrolyte parameters and special leveling additives together with strong reverse pulse plate have enabled a new production technique „Super Filling" of blind micro vias. With this technique dimple values less than 10 µm are achieved with the minimum of copper plating on the panel surface. Figure 9 shows plating results achieved with a blind micro via diameter 170 µm and depth 100 µm, the dimple in the copper plating is less tan 10 µm with a plated copper deposit of only 15 µm.

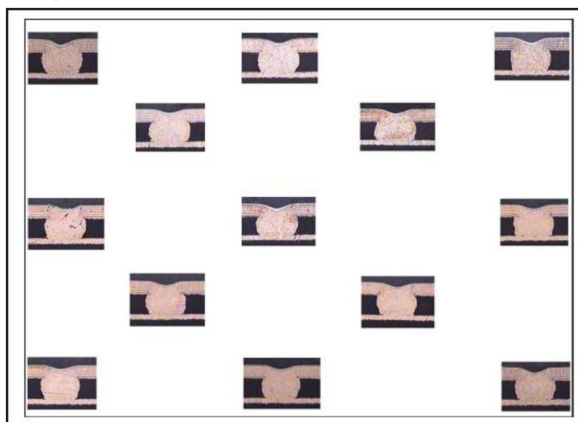
Figure 9: *"Super Filling" achieved with blind micro via electrolyte*

Filled blind micro via Diameter 170 µm Depth 100 µm
Surface copper plate 15 µm



The electrolyte used is designed to fully utilise the strong reverse pulse parameters whilst giving a smooth deposit which meets reliability requirements. For all blind micro via filling systems the copper plated surface distribution must be optimal to ensure low dimple at the same time as a low copper plated thickness. Even a surface variation of 2.5 µm on the surface can cause a dimple variation of up to ±5 µm which would give an unacceptably high quality variation. Figure 10 shows the variation in blind micro via filling in panel plating application with a horizontal Inpulse system.

Figure 10: *"Dimple" distribution assessed by micro-section of blind micro vias over panel surface.*

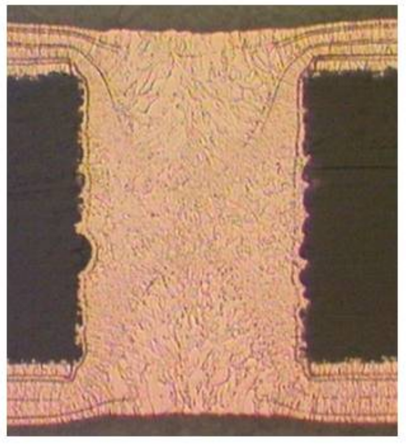


Use of copper filled through hole plating for production of plugged cores.

The “super” filling technology can be used to fill through holes with plated copper, an example of this is shown in figure 11. The through hole is in a foil 150 µm thick with hole diameter 120 µm.

Figure 11: *Filled through hole using “Super Filling” technology*

Foil thickness 150 µm
Hole diameter 120 µm
Plated copper 24 µm
Dimple < 10 µm



Use of plated copper to fill through holes will have significant impact on the thermal characteristics of the completed HDI package with core together with filled blind micro vias.
It is also possible to use the filled through hole technology to replace filled blind micro via production in some cases. For example a blind micro via with diameter 100 µm in a foil 60 µm thick with 5 µm copper clad can be made as a filled through hole which would enable savings in laser drilling costs together with potential productivity increase.

Summary

The use of insoluble anodes gives an assured production of a well defined copper plated surface which is ideally suited for HDI production for either hand held devices or IC substrate. An added advantage is the inherently stable electrolyte system which gives long blind micro via fill life time in both horizontal and vertical plating equipment.
The “Super Filling” technique takes the basic via filling system used in horizontal Inpulse equipment together with a correctly adjusted electrolyte to enable uniform blind micro via filling with less than 10 µm dimple and only 15 µm copper plating. This new development enables production of 50 µm line and space with panel plating with the advantages of the best possible surface distribution.
This use of thin panel copper plating is being investigated as a variation in the semi-additive process for IC substrate production. In this the electroless copper deposited on the whole panel is first reinforced with electrolytic copper before image step followed by blind micro via filling. The limiting factor in this development is the capability of the flash etch or whether a plated etch resist can be used.

References

[1] S. Kenny and K. Matejat “*HDI production using pulse plating with insoluble anodes*” EPC 2000 Proceedings of the European PCB Convention.
[2] J. Barthelmes “*Filling of Blind Microvias Theory and Application*” Plus 2001.