Electrolytic Solder Deposit for the Next Generation Solder Resist Openings and Bump Pitch

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Abstract:
Current methods for the formation of pre-solder bumps for board to board solder joints and in particular for flip chip attachment use stencil printing techniques as part of the process utilising a suitable solder paste. The continuing trend towards increasing miniaturisation and the associated decrease in size of solder resist opening, SRO is causing production difficulties with the stencil printing process. Practical experience of production yields has shown that stencil printing will not be able to meet the requirements for solder bump pitch production below 0.15 mm for IC substrate applications and also 0.3 mm bump pitch for HDI applications.

This paper describes a novel approach to replace the stencil printing process by use of an electrolytic deposition of solder. In contrast to stencil printing, use of electrolytic deposition techniques allows production of solder bumps with a pitch below 0.15 mm and with a SRO below 80 µm.

The process steps required for electrolytic deposition of solder bumps are shown together with the necessary pre-treatment, this includes metallisation techniques to enable uniform solder deposition over the bump array.

The advantages of replacement of stencil printing by electrolytic solder deposition are shown and in particular the improvement of bump reliability and the potential to significantly decrease costs by yield improvement.

Introduction

At the introduction of flip chip technology by IBM in the early 1960´s these devices were mounted on a ceramic substrate where thermal expansion mismatch between the silicon chip and the ceramic substrate is less critical. In comparison with wire bonding technology, flip chip technology is better able to offer higher packaging density and higher electrical performance due to shorter possible connections and lower inductance. On this basis flip chip technology has been used for the past 40 years using high-temperature soldering of the controlled-collapse chip connection, C4 to the ceramic substrate. In recent years, driven by the demand for high-density, high-speed and low-cost semiconductor devices for modern electronic products, use of flip chip devices mounted on a low-cost organic circuit board has experienced a rapid growth.

In the current low-cost flip chip technology, the top surface of the semiconductor integrated circuit (IC) chip has an array of electrical contact pads. The organic circuit board has also a corresponding grid of contacts. The low-temperature solder bumps or other conductive adhesive material are placed and aligned in between the chip and circuit board. The chip is flipped upside down and mounted on the circuit board in which the solder bumps or conductive adhesive material provide electrical input/output (I/O) and mechanical interconnect between the chip and circuit board. For solder bump joints, an organic underfill encapsulant is typically used in the gap between the chip and circuit board to constrain thermal mismatch and lower the stress on the solder joints.

In general for flip chip assembly by solder joints, the metal bumps, such as solder bumps, gold bumps or copper bumps, are commonly pre-formed on the pad electrode surface of the chip. The corresponding solder bumps typically using a low-temperature solder, are also formed on the contact areas of the circuit board and after reflow the chip is bonded to the circuit board by means of these solder joints.

The most common method for formation of presolder bumps on the circuit board is with the stencil printing method of a suitable solder paste, however current practical experience has indicated that this method is reaching practical limits. Reduction of bump pitch to below 0.3 mm together with reduction in solder resist opening diameter is causing increased yield losses. In figure 1 the projected development of solder resist opening (SRO) is shown together with the limitation at 80µm SRO diameter for production of IC substrates.

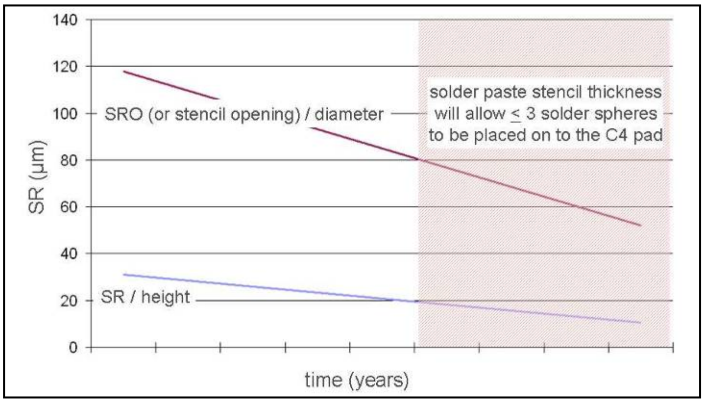


Figure 1: Projected development of SRO and SR height with technology barrier at 80 µm SRO

As an alternative technology solder bumps deposited by the electroplating of a suitable metal or alloy can meet the demands in reduction of solder bump pitch also below 0.15mm, a multi-step electrolytic process to form solder bumps on an organic substrate is described in reference 1. This process describes preparation of the surface by deposition of a seed layer onto the solder mask, the solder resist opening is then defined by a resist layer and the metal solder bump is then formed in the opening by electroplating. Subsequent removal of the plating resist and also the seed layer is necessary to leave the completed solder bump.
The solder bump is deposited as a tin or a tin alloy material which is then reflowed after processing. Figure 2 shows the surface view of tin solder bumps after reflow.

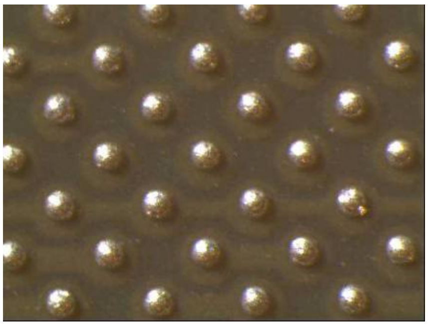


Figure 2: Electrodeposited solder balls on SRO 80µm after reflow

The deposition of solder bumps as described in reference 1 requires the use of a photo resist to define the area for metal deposition. This process in itself suffers from yield issues particularly when used for the definition of fine dimension structures. The latest process for electrolytic solder bump deposition can eliminate this by the use of an innovative tin filling process which can preferentially deposit tin into the SRO.

Developments and latest results in tin solder filling.
Figure 3 shows a schematic of the pre-treatment used for the tin filling process. The solder resist is processed with a seed layer to allow electrolytic deposition followed by processing in the solder bump process, an optional barrier layer may be used in this sequence.

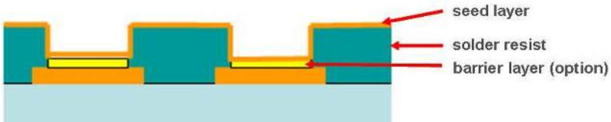
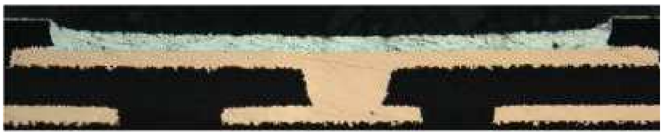


Figure 3: Schematic of process sequence for solder bump processing.

Due to the preferential deposition of tin in the SRO a minimum of metal is deposited onto the surface of the substrate, this is then removed by use of a differential etching process which will leave the completed solder bump. Figure 4 shows microsection data of plated structures which were processed with tin filling.



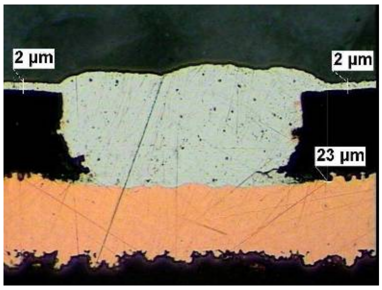


Figure 4a: FCBGA structure with SRO 400 µm. 4b: Solder filling of 23 µm structure

With this process the use of an imaging step is not necessary which gives process savings together with potential yield increase due to elimination of processing steps.

Summary

The solder filling process has been evaluated for use in HDI applications as well as for IC substrates. The method for production of solder bumps can meet the demands for varying SRO sizes whilst maintaining a constant deposit thickness. A number of processing steps may be eliminated depending on the production sequence chosen. Latest results show a tin solder deposit thickness variation of ± 10% plated over the whole panel surface.

References

1. U.S. Pat. No 7,098,126 (H.-K. Hsieh et al.) Formation of electroplate solder on an organic circuit board for flip chip joints and board to board solder joints.