Via filling applications for IC Substrate and in particular Flip Chip BGA

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Introduction

IC substrate fabrication has been relying now for several years on the formation of Blind Micro Vias (BMV) as connectors between different layers. These BMVs are Cu plated and usually completely filled to improve the reliability of connections between different Cu layers compared to the traditional conformal plating. The complete filling enables direct stacking of BMVs (Fig 1 right), a further approach to miniaturize features on the IC substrate. Especially BGAs could be reduced in spacing by leaving away the extra contact pad which was required.

Fig 1. Blind Micro Vias completely filled with electrolytic Cu, right: stacked BMV

These filled BMVs are usually produced by a built up technology (SAP) using traditional vertical Cu plating lines with soluble anodes. In the past several drawbacks and limitations of this technique have been reported: (i) short life time of electrolytes (weeks to months) , (ii) surface distribution of plated Cu inferior to inert anode systems and (iii) limitations in filling performance if the plated Cu thickness is below 15 µm (0,6 mil). The last point is important the next generations of Chip carriers which will see only 10-12 µm or less of plated Cu.
This report describes the progress in the plating technology to meet future and current demands from a process technology point of view. We will also present a new production technology by using embedded conductors based on the improved Via filling technology.

Conventional DC plating systems with soluble anodes

This is the process of record for most suppliers of IC substrates. Comparably short life time of the Blind Micro Via electrolytes have been reported by several authors leading to substantial cost increase and It is supposed that special intermediate chemicals are formed only at the soluble Cu anodes which are detrimental for the filling process. Since intermediates are built out of a basic additive of all via filling electrolytes it was not possible to exchange that additive. Normally, two components the so called leveller and brightener are added. Both additives have several constituents.
Our approach was to mask the detrimental effect by using other already existing additives. After introduction of a third component for replenishment we now see life times of more than half a year even a year. This is major step in process control and has been further improved by introduction of an analysis method for the third component. Fig 1 shows an x-section through a IC substrate produced by this technology.

At the moment, IC substrates with dimensions below 15 µm (0,6 mil) lines and spaces are under evaluation at several producers. Surface distribution (Cu thickness variation) values of 10-12 ± 3 µm are desired while Blind Micro Vias of 60 x 40 µm² dimensions (2,4 x 1,6 mil²) have to be

completely filled. This new demand could lead to change in the production technology. For these new demands we are developing new systems based on dimensionally stable anodes (DSA).

Dimensionally Stable Anode systems

These anodes are covered with an inert Iridium oxide or a mixed Tantalum/Iridium oxide layer and used since several years in plating technology. The big advantage of such a system is the fixed size of the anode generating a more regular current distribution. Replenishment of Cu is done either by dissolving Cu oxide or pure Cu with the aid of Fe(II)/Fe(III) redox couple in the electrolyte. The latter system is used by us to further improve the Cu Via filling.
Compared to soluble anodes systems we definitely see an improvement of Cu thickness distribution. Especially the differences between thin 10-15 µm and larger 25-40 conductor lines can be minimized.
A system based on DSA has been recently introduced and is able to fill Blind Micro Vias of 70 x 40 µm² (2,8 x 1,6 mil²) with 13 µm (0,52 mil) or less as depicted in fig 2.

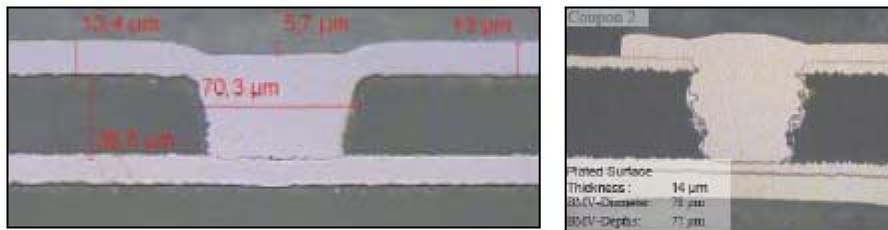


Fig. 2: Left: BMV filled in a IC substrate with Inplate DI2 system based on DSA. BMV: 70 x 40 µm². Right: HDI board: 78 x 77 µm² BMV filled with only 13 –14 µm Cu

Conveyorized Reverse Pulse Plating systems

A further improvement can be achieved by using conveyorized lines which generate exactly the same surface distribution for each panel. The panel to panel variation is minimized.
Our Uniplate ™ system is a combination of horizontal conveyorized desmear, e'less and electrolytic plating modules with controlled flood/spray system and individually controlled RPP rectifiers to enable Cu plating within ± 10 % (min-max) range. A surface distribution which cannot be met by hoist type machines.
The plating line combines electrolytic plating and at the same time etching with Fe (III) in the same electrolyte. The Fe ions are not co deposited into the layer but simply etch the Cu preferentially from the surface during plating. The etching speed is different for surface and via bottom so that a net etch effect for only the surface results. We call this process SUPERFILLING. It leads to a substantial reduction of plated Cu by about 30-50 % while filling the BMV completely. With this technology we are confident to meet future demands for IC substrate manufacturing.
Fig. 3 shows examples of filled BMVs plated with this Inpulse technique. (**In**ert anodes with Reverse **pulse** plating). Even larger BMV can be filled with less than 13 µm Cu.

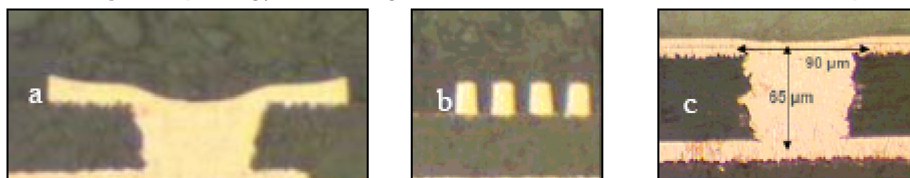
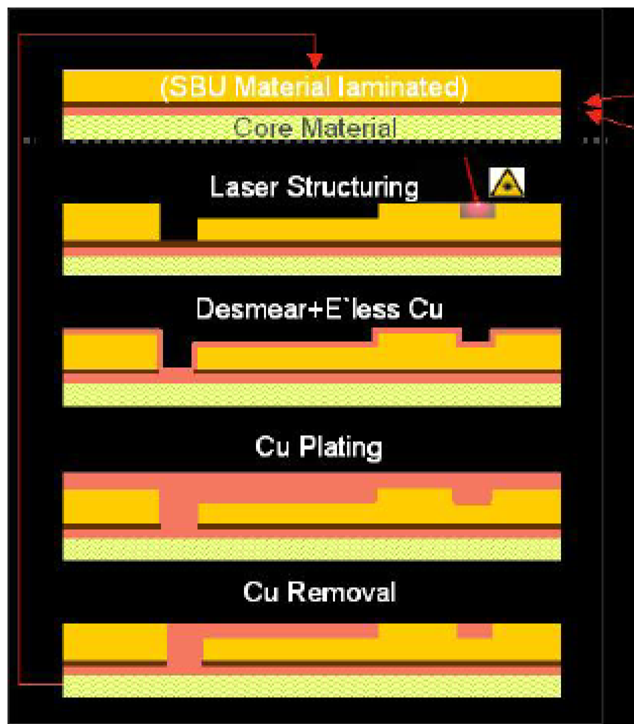


Fig 3: a+b) Filling BMV (70 x 40 µm²) and plating 10 µm l/s. c) Filling of large BMVs , 90 x 60 µm² (3,6x2,4 mil²) with only 12 µm (0,48 mil) Cu .

A novel approach for IC substrate manufacturing (Via² or LEC)

A new process which is mainly based on good structure filling performance shall be introduced here. It is aimed at the production of IC substrates with dimensions of lines and spaces below 15 µm (0,6 mil). There are different names for this process like Via² or LEC, Laser Embedded Conductors, but the concept is the same. Fig. 4 shows the general process sequence.



Adhesion promoter
Cu Core inner layer

Fig. 4 . Process sequence for the manufacture of laser embedded conductor.

1. SBU material lamination on core substrate
2. Laser structuring into SBU material
3. Desmear and e'less Cu plating
4. Electrolytic Cu Plating
5. Etching of Cu
6. Restart at 1. (SBU lamination) to produce a new layer on top

It starts with the lamination of a SBU material on a core. The core might be treated with an adhesion promoter. Then the laser is used to ablate the SBU material and form trenches, pads and blind micro vias (BMV) the latter having a connection to the core Cu layer. The so formed embedded structures need to be desmeared before further treatment and made conductive by an e'less Cu step. After this the complete filling of all structures by electro plating has to be achieved. The following etching step generates the circuitization. The process might be continued with lamination of a new SBU layer and the aforementioned steps to generate a multilayer.
This sequence deviates substantially from the traditional circuitization process based on a photo resist application by eliminating the latter completely (passivation, lamination, imaging, developing, stripping). But to realize that process some obstacles had to be overcome.
It starts with the laser performance. In the past ablation speed of common lasers was not competitive to meet the through put demand but latest developments brought substantial progress. Nowadays, there a pulsed ns or even ps laser systems available which ablate a complete IC substrate panel (500 x 500 mm² or 19,7 x 19,7 inch²) in less than 3 minutes with lines and spaces below 10-15 µm (0,4-0,6 mil). Fig. 5 shows a SEM picture of pads and conductor lines in a common SBU material.

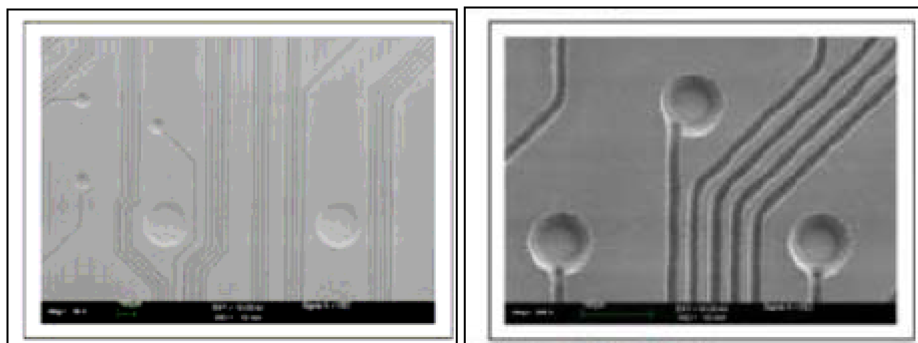


Fig.5 SEM of laser ablated structures in common SBU material. Pads (90 and 250 µm = 3,6 and 10 mil diameter) conductor lines (15 µm = 0,6 mil). Structures are 25 µm = 1 mil deep.

The following desmear process removes particles and smear from the ablation process and prepares at the same time the surface to increase the peel strength of the embedded Cu

structures. Desmearing is another critical process step since it alters the shape and size of the trenches. Fig. 6 shows the influence of desmear intensity on the track width and shape.

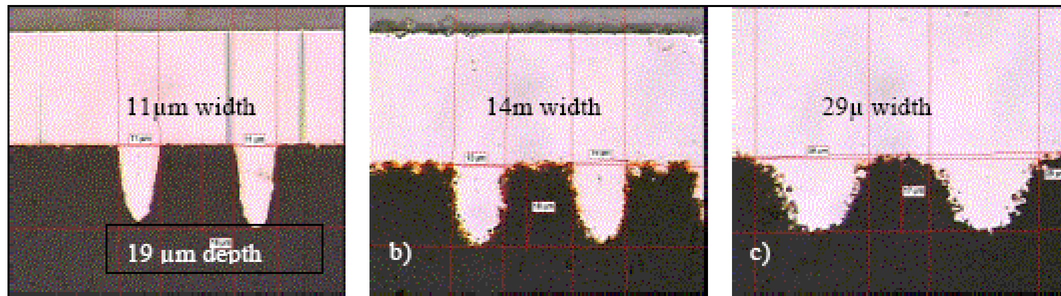


Fig 6 : Trenches a) directly after laser ablation, b) after mild desmear and c) after strong desmear. All trenches are plated with Ni layer for better contrast.

The desmear process can be successfully conducted under conditions of b) with sufficient roughening and still acceptable loss in material. The line width increased from 11 to 13-14 µm with insignificant depth reduction. The SBU materials normally consists of filler particles which, after removal during desmearing, leave holes of at least the same size. Thus SBU materials with particles sizes below 1µm (0,04 mil) are preferred. The smaller the size the better the resolution!
On this so prepared material e'less and electrolytic plating is conducted. For both, the e'less and electrolytic plating processes, the surface distribution is the most important parameter to control. It is absolutely necessary to achieve the best possible Cu distribution since the subsequent etching process is significantly affected. Thus, processing should be performed in a conveyorized system since these systems have the lowest possible panel to panel variation. All our tests have been conducted in our Uniplate ™ system.
On these panels BMVs, tracks and pads of very different sizes have to be completely filled with a minimum of Cu on the surface. Dimples of pads or BMV should be minimized and not vary over a panel. To achieve a minimum of Cu thickness we used the above mentioned SUPERFILLING process by plating Cu onto the surface and into trenches and Vias while etching preferentially the surface.
Fig. 7 shows a combination of tracks and pads on one x-section after plating 19 µm Cu in an earlier attempt. It is obvious that the smaller tracks are completely filled without any resulting dimple. The wider the structure the deeper the resulting dimple remained. Pads of different size had usually a dimple in the range of 6-9 % of the pad diameter.

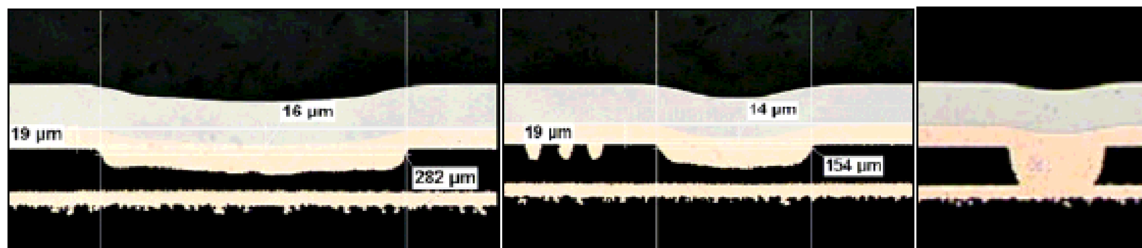


Fig. 7: Early attempt to fill pads, BMVs and trenches after desmear, e"less and electrolytic Cu plating in hor. converyorized Uniplate system. Ni plating on top to enhance contrast in X-sections.

It is obvious that pads are more difficult to fill than BMVs. This was a general observation and is mainly based on the fact that the filling mechanism is based on different transportation speed of additives into features. A shallow pad has a very different diffusion layer than a BMV or a pad. Thus, the wider and shallower a pad the more it behaves like a surface.
Since that early attempt the plating performance has been further improved. Remaining dimples for a standard process are now in the range of about 3-4 % of the pad diameter.

Fig. 8 Showing improvement on pad and BMV filling with smaller dimples: for 280 µm (11,2 mil), 200µm (8 mil) pad and 130 µm (5,2 mil) BMV. 22 µm (=0,9 mil) Cu on the surface.

Further improvements can be expected by designs changes. Latest designs do not need any pad structure anymore and consist of trenches and Vias only. These structures are comparably easy to fill with significantly less Cu and and little dimples. Small trenches (10-15 µm = 0,4-0,6 mil) can be filled with only 5µm (0,25 mil) Cu or even less!
Latest trials in our TechCentre showed a further improvement which resulted in completely or even overfilled BMVs and pads. So far, these results are not transferred into a "ready to use" industrialized process yet but further work is under way.
The following etching step can only be applied if the remaining dimple is minimized or even absent, otherwise a combination of a mechanical and chemical etching procedure is necessary to level differences in the Cu thickness.
Fig. 8 demonstrates the applicability of an etching step for a nearly perfectly filled structure.

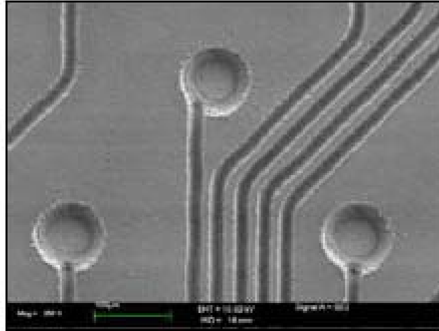


Fig. 8 Pads and trenches after laser ablation, and after complete circuitization.

The above described process has been applied for demonstrators and is under qualification. Several benefits of this new process have been identified :

1) Less process steps with less failure possibilities
2) Applicability to features below 10-15 µm(0,4-0,6 mil)
3) Higher process stability due to embedding tracks (higher "peel strength" of Cu)
4) Layer reduction possible since ground and signal can be put on same layer due to higher laser accuracy

In further tests it has been shown that a superior electrical performance can be achieved due to the higher laser accuracy compared to conventional routing process.

Summary:

Latest developments in Cu filling of small features (BMVs, trenches and pads) have been significantly improved the process stability for manufacturing IC substrates. Techniques to overcome instabilities as short electrolytic bath lives have been developed. Moreover, substantial improvements in the via filling quality have been achieved by applying conveyorized Reverse Pulse Plating technologies. This technology in conjunction with Superfilling™ has significantly reduced the amount of necessary Cu to fill structures. From a process technology point of view we can see an improvement in the sequence

soluble anodes, hoist type, DC → DSA, hoist type, DC → DSA, conveyorized, RPP (best)

Since the latest technology can also be applied to fill shallow features as pads and thin conductor line at the same time it opens the way for a new circuitization process, known as LEC or Via². This process, based on laser embedded structures, offers the possibility to produce smaller features (lines and spaces below 10-15 µm = 0,4-0,6 mil) while reducing the necessary layers. The process is currently under qualification.

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