Electrolytic Solder Deposit for Next Generation Flip Chip Solder Bumping

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Introduction

Current methods for the formation of pre-solder bumps for flip chip attachment use stencil printing techniques with an appropriate solder paste. The continuing trend towards increasing miniaturization and the associated decrease in size of solder resist opening, SRO is causing production difficulties with the stencil printing process. Practical experience of production yields has shown that stencil printing will not be able to meet future requirements for solder bump pitch production below 0.15 mm for these applications.

This paper describes a novel approach to replace the stencil printing process by use of an electrolytic deposition of solder. In contrast to stencil printing, use of electrolytic deposition techniques allows production of solder bumps with a pitch below 0.15 mm and with a SRO below 80 µm.

Methods for production of electrolytic solder bumps based on Sn/Cu are shown and in particular a method to control the alloy concentration of electroplated tin/copper bumps. Test results are presented together with comparison of the advantages and disadvantages.

The general advantages of replacement of stencil printing by electrolytic deposition of solder bumps are shown and in particular the improvement of bump reliability and the potential to significantly decrease costs by yield improvement.

Pure tin deposits by panel or pattern electroplating

Prerequisite for the deposition of a tin based solder is the ability of solder electrolyte system to completely fill recessed structures like solder resist openings, Blind Micro Vias etc. Common tin electrolytes e.g. which are frequently used as metal resists in patterning PCBs and IC substrates do not fulfil this requirement. For this very specific task a new generation of acidic tin and tin alloy electrolytes had to be developed.

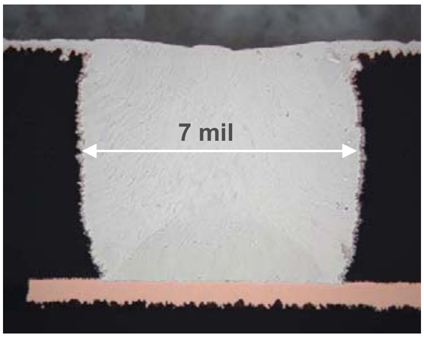

Fig. 1 is a good example for the extreme levelling effect of such a new tin electrolyte. A Blind Micro Via with dimensions of 150 µm x 180 µm (6 mil x 7 mil) is completely filled with pure tin within only 15 min and 6-7 µm Tin on the surface. This striking fill up performance is not only restricted to pure tin but can also be observed for Sn/Cu systems as we will show later on in this publication. Ternary systems have not been investigated so far due to the fact that an effective control of such an electrolyte systems is difficult if not impossible for IC substrate manufacturing.

Fig. 1: Electrolytically Tin filled BMV (6 mil x 7 mil) with the new SolderfillTM process

With the outstanding fill up performance new process applications and processes are viable. Fig. 2 shows two possible sequences, one of which uses a patterning process known from standard IC substrate technology (a) whereas the other one is based on full panel plating process (b)

Process sequence (a) may result in a direct solder ball formation after reflow whereas process (b) can be used to plate the basis either for solder balls or the connection to solder studs from the chip itself.

Process (a) is applicable where µ-ball solder placing has its limitations. Solder ball dimensions of less than 100 µm (4 mil) are possible with so far no limitations towards smaller dimensions at least for the electroplating step. Most of the involved processes steps before the electrolytic solder depot require techniques which are available in the current IC substrate industry. The only exception is the application of a photo resist on a solder resist opening.

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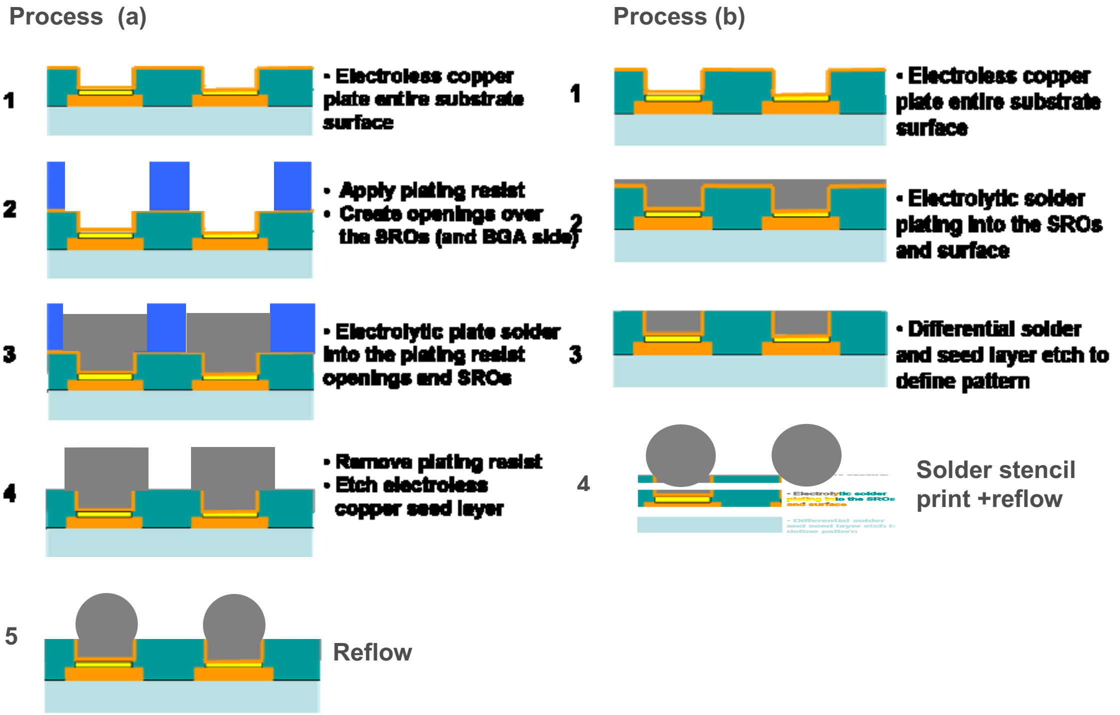

Fig. 2: Possible process flows for electrolytic solder deposition in pattern (a) (left) and panel plating (b) mode

Here, alignment of photo resist and solder resist opening is a crucial step. We have seen in first attempts many examples for displacements larger than half of solder resist opening. In that case it will become difficult to achieve a reliable process. Slight mismatches can be accepted since solder tends to self align during the reflow process. Fig. 3 shows an example for such a self aligning effect. The Sn based solder deposit has not been ideal due to the lateral off-set between the underlying solder resist opening and the photo resist on top of it. The photo resist has already been stripped in fig.3 so that only the asymmetric deposition of the tin itself can be seen. The reflow results in perfectly symmetric solder balls.

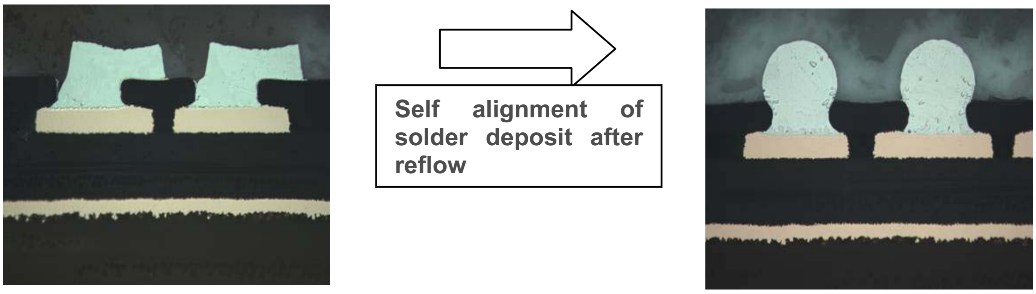

Fig. 3: Self aligning of a solder deposit after reflow

Besides the benefit of overcoming dimensional limitations in solder ball placement the SolderFill process also eliminates the need for a final finish as immersion Sn or Ag, since Tin and Tin alloys can be directly plated on the underlying Cu.
Moreover, it is possible to plate many different sizes at the same time so that this process can be used simultaneously for both the C4 side and the BGA side of an IC substrate. On the BGA side only a conformal solder deposit of 5-7 µm is needed. This layer replaces the usual final finish and serves as the basis for the subsequent solder printing step.

Process (b) does not require any alignment process and seems to be at first glance easier to realize than process (a). The benefit of such a panel plating process compared to a pattern

plating process is usually a perfect thickness distribution of the deposit over a whole work piece like a PCB or a IC substrate panel. On the other hand it requires the development of a completely new wet chemical process step, the differential etch of the solder layer, may it be Sn or Sn/Cu. This differential etch must be able to attack preferentially the deposit on the planes without dissolving too much of it from the solder resist opening. Otherwise, it might be difficult to effectively control the amount of the solder itself. The difficulty in this step lies in the fact that the deposit on the surface is a mixture of the solder material itself and the seed layer deposit which includes Cu and traces of Pd. So far, no current product on the market is able to fulfill this requirement. Work on this topic is ongoing in our group and we believe that we will come up with a solution in due course.

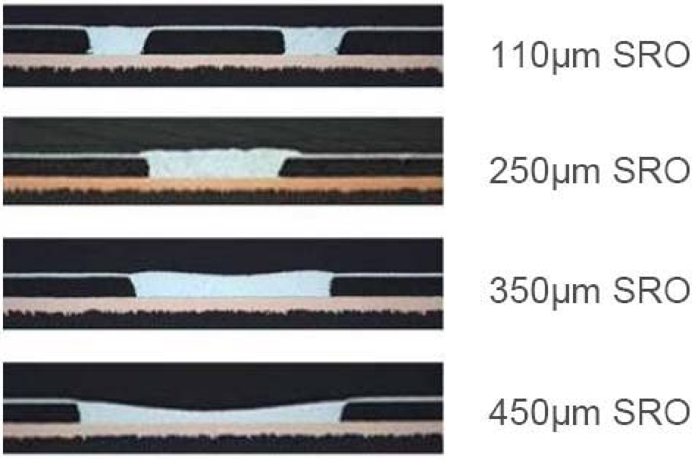

Fig. 4: Examples for the electrolytic SolderFill process with an overall Sn thickness of 5 µm on the surface for various sizes of SRO.

The most likely application for this panel plating process would be the formation of the solder ball basis instead of the formation of a complete solder ball. This is an attractive option. According to IC substrate manufacturers it becomes increasingly difficult to place the solder balls into recessed structures without voiding. The placement of solder balls on a plane surface would be much easier and the failure rate is expected to drop significantly. It would enable the industry to extend the use of the current ball placing technology of solder. Limitations for such a process are related so far with the ability to fill up a solder resist opening completely. Fig. 4 shows a test series of different dimensions. From these results it becomes obvious that resist openings of 450 µm and larger are so far not accessible.

The aforementioned limitations favour the pattern plating process (a) and the following investigations are related to this process flow. As we will see later on this is also the process which has been put forward so far by the industry

Sn/Cu Deposits

The deposition of a pure Tin from methane sulfonic acid (MSA) based Sn electrolyte into a recessed structure would not result in a pure Sn solder! This is simply due to the fact that a) the seed layer process and b) the basis in a solder resist opening under the deposit are usually made from Cu. Since Cu and Sn diffuse into each other the resulting deposit is a Cu/Sn alloy rather than pure Sn. This diffusion process is fast especially if heat is applied as it is the case during the reflow process. Moreover, formation of an intermetallic phase built up by a Cu rich Cu_3Sn and and Sn rich Cu_6Sn_5 species is observed but this only at the contact to the capture pad. It is essential to clarify to which extent the underlying Cu influences the solder characteristics and if this can be influenced by the process itself. Therefore, a calculation of the theoretical composition of the solder deposit has been done.

If one assumes that the Cu from the resist opening walls will completely diffuse during the reflow and the same amount of Cu from the basis will also diffuse one can roughly calculate the percentage of Cu in the Sn/Cu deposit. This has been done for a 50 µm wide solder resist opening with a 80 µm wide photo resist opening on top and 45 µm thick Sn deposit. The thickness of the seed layer can easily be controlled within a ± 0,05 µm range so that variations in the Cu content will be less than ± 0,25 %b.w.. From this admittedly simplified consideration it seems to be possible to produce an eutectic or near eutectic Sn/Cu deposit with a content of 0,7 % Cu as it is used today.

Seed layer µm	**0,1**	**0,15**	**0,2**	**0,4**
Cu cont. % by w.	**0,5**	**0,75**	**0,9**	**1,8**

Tab1. Theoretical constitution of a 45 µm thick Tin deposit after reflow as a function of the Cu seed layer thickness. Process (a) with following dimensions: SRO 50 µm width and 25 µm depth, Photo resist 80 µm wide and 20 µm depth.

Not only the content but also the distribution of Cu in Sn is of major importance. We have investigated FIB cuts by SEM to prove that Cu is evenly distributed all over the solder ball after the reflow process. This is depicted in fig. 5.

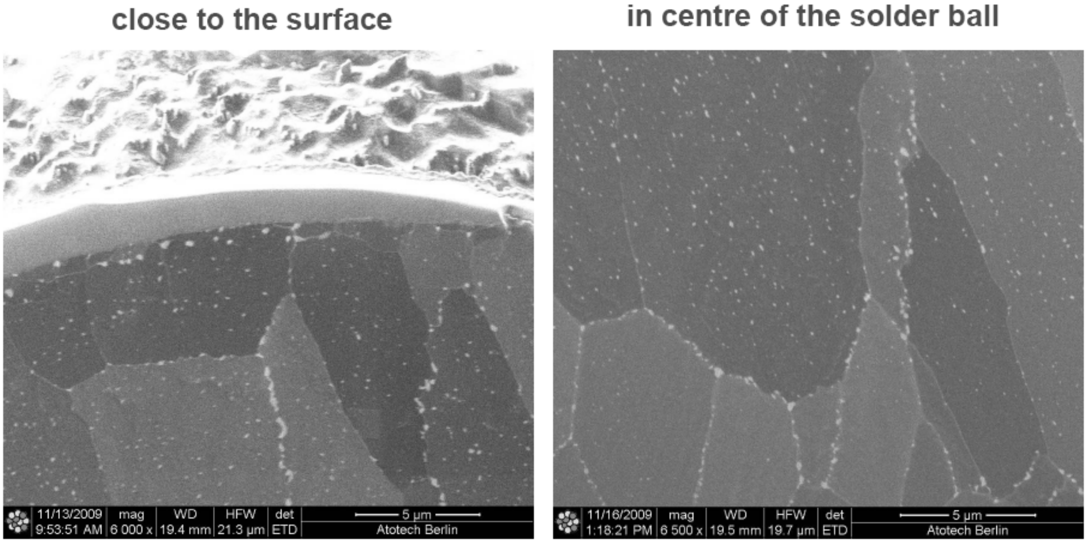

Fig 5. distribution of Cu (white spots) in the Sn/Cu deposit after reflow.

Further element mapping studies of such plated solder ball confirmed the even distribution.
The intermetallic phase formation at the boundary to the capture pad has also been in our focus. Our investigation showed a regular formation of both Cu_3Sn and Cu_6Sn_5 phases with no surprises. Further details on this topic will be given in the full paper.

Reliability investigations

Reliability investigations on the aforementioned electroplated solder system are scarce simply due to the fact that this is not in IC substrate production yet. Qualification for Sn/Cu system at a customer is underway and table 2 shows a summary of a number of successful tests

Tests Parameters	**Parameters**	**Status**
TCT	**55°C→125°, 1000 cycles**	**Passed**
Pressure Cooker Test	**100 % RH, 121 °C**	**Passed**
HTST	**150 °C1000h**	**Passed**
HAST	**85%RH, 130°C, 3,5 V 200 h**	**Passed**
Cold Ball Pull	**0,21 mm&s**	**Passed**
Ball Shear	**5 mm/s**	**Passed**
Mult reflow	**260°C**	**Passed**
Thermal stress	**288°C**	**Passed**

Table 2: Passed test for an electroplated Sn/Cu solder deposit after assembly

Summary

We have shown two different ways to use electrolytic methods for SnCu solder deposits. A pattern plating process using photo resist technology has been used to characterize the deposit of SnCu and qualify this for production of IC Substrates. A number of reliability tests for an IC substrate with the Sn/Cu solder were passed successfully

If this systems will be successfully adapted remains open. This may depend strongly on different applications and infrastructure at suppliers. Nevertheless, electroplating solder systems are well suited to overcome problems with the existing solder ball technology for small solder resist openings such as 100 µm or less. The electroplating technology is not restricted in this respect, it may even become easier to fill solder resist openings the smaller they get. In contrast, larger SRO > 400 µm are difficult to plate. But in that case the existing screen printing technology has no problems.

We have shown that for IC substrates both sides, the C4 and the BGA side can be plated in one step, plating a full solder ball on the C4 side and a solder basis on the BGA side. The process does not require a final finish as it is the case in current technology and offers therefore an additional cost benefit. We believe that both the technological as well as the economic benefits are good reasons for introduction of the process. There are many open questions up to this point mainly related to reliability. The existing solder technology is based on thousands of different reliability investigations and specifications. We do not know as to which extent electroplated solder must fulfill the same specifications as solder pastes. We need to answer the questions of controlling solder constitution and to which extent it is necessary.

Acknowledgements

Without the help of the following people (in alphabetical order) we would not be able to show these results:

Adam Chen (Atotech Taiwan), Nina Dambrowsky, Sengül Karasahin, Thomas Pliet (All Atotech Germany).