

Influence of Electroless Copper on IC Reliability

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Abstract

The process of plating through holes (PTH) is inherent to modern PCB manufacturing. In an arena of increasing circuit density and layer counts, the reliability of the PTH process is under constant microscopic examination. The aim of electroless copper is to plate a conductive layer through a hole or into a blind microvia. In this context an interconnect (IC) refers to the copper to copper adhesion within the functional constraints of a circuit board. As these can include many inner layers, the interconnection quality is of prime concern. In addition the PTH process also inherits the issues from the preceding manufacture.

Some examples are highlighted below:

Base material

Material properties can result in significant Z axis mobility. Hybrid builds (different materials in one build) can be exceptionally vulnerable and the problem is amplified in thicker panels.

Drilling

Drilling practices can affect smear residues and inner layer damage dramatically. Later processes can minimize the impact of these but only if the manufacturer is aware of it.

Unless the source of a type 1 inter-connection defect is clear, it is usually attributed to the PTH process employed.

Using electroless copper as an example, the impact of PTH on IC quality will be discussed. For this purpose it is useful to divide the PTH process into the following subsets:

- Desmear
- Cleaning/Conditioning
- Activation
- Electroless copper

This paper presents the impact of the individual PTH steps!

Background

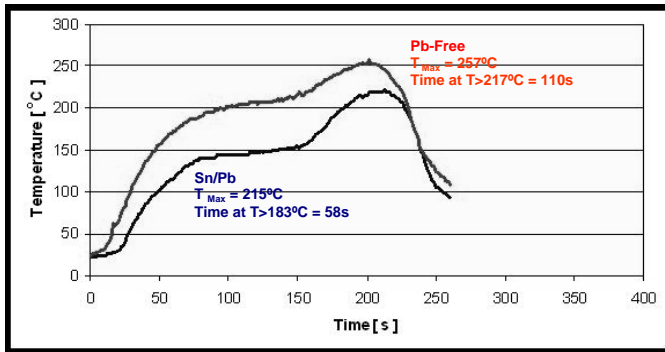
PCB manufacturers must permanently contend with difficulties associated with production of PCBs with ever more complex designs, technology requirements and increased lifetime/reliability requirements. A good example of this development is the increased use of electronics in new applications such as in the automotive industry, where PCBs are being exposed to very high temperatures in such environments as car engines or braking discs.

Issues pertaining to the laminate material used, via sizes, copper layer thickness and electrical requirements, which significantly affect the manufacturing process are often the prerogative of PCB designers with extremely limited if at all any consultation with manufacturers.

Most importantly introduction of the Restriction of the use of Hazardous Substances (RoHS) directive in Europe from July 2006, has obliged PCB fabricators to employ RoHS compliant materials and processes. RoHS affects the metals Lead, Mercury, Chrome (VI), and the bromine containing resins PBB and PBDE, which have to be under 0.1% w/w in the finished product as well as Cadmium that has to be under 0.01% w/w.

In compliance with RoHS, new lead-free soldering processes mainly those based on Sn/Ag/Cu (SAC) alloys have emerged. These have melting points that are about 30 °C above that of the conventionally used Tin Lead Alloy (Sn63Pb37). A comparison of the different assembly temperature profiles shows that lead free soldering, not only results in higher temperature but also results in longer exposure at the higher temperature. This combined effect results in significantly higher thermal stress of the base material and consequently for the copper deposit as well.

The following graphic shows the temperature profiles for lead free soldering versus traditional lead containing solder:



New base materials with alternative fire retardants have also resulted from the halogen ban imposed by RoHS. These typically employ hardeners that are used in combination with multifunctional epoxy resins to provide better temperature stability and lower Coefficients of Thermal Expansion (CTEs). Another typical trend for these materials is the inclusion of filler materials mainly to reduce CTEs as well as to enhance other physical characteristics. These new materials have the ability to withstand high temperatures for longer periods of time before delaminating as well as having significantly reduced CTEs than their predecessors.

In spite of these improvements to the base materials, it still remains imperative to adapt the electroless copper deposition process if the elevated challenge of achieving good copper to base material and electroless to acid copper interconnection is to be met.

Using results from an R&D project and experiences from customer process adaption within the company Atotech, the process steps and parameters that have the most influence on the appearance of interconnect defects (ICD) will be briefly described.

Note

It is important to always bear in mind that the base material and quality of lamination have an overriding influence on ICD performance compared to electroless copper.

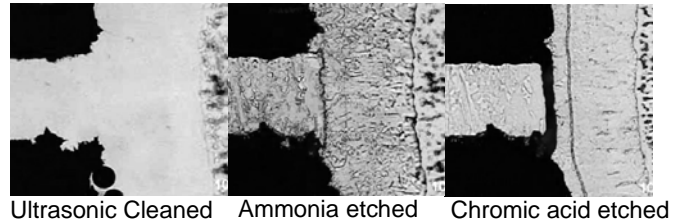
EVALUATION METHODS

TCT (in accordance with IPC –TM-650 Method 2.6.7.2A) and IST (according to IPC –TM-650 Method 2.6.26) are the two most common methods used to evaluate interconnect reliability. Most Japanese OEMs also require hot oil testing (JIS C5012). These methods are intended to mimic the thermal stress the copper layers will be exposed to later, when they are used in the final products.

Solder shock testing on the other hand is used to test interconnect reliability with respect to thermal stresses endured during the production process especially the soldering process. During the R&D project from which most of the experiments in this paper are taken, thermal

shocking was additionally conducted at 326 °C to cater for the elevated temperatures of Pb-free soldering. All evaluations of micro sections were carried out after ultrasonic cleaning, prior to etching. This is because after etching separation lines between copper layers become visible and it is then difficult to tell if these are the result of a real separation at the copper-copper interconnect.

The following pictures show cross sections of an inner layer contact with no ICD:

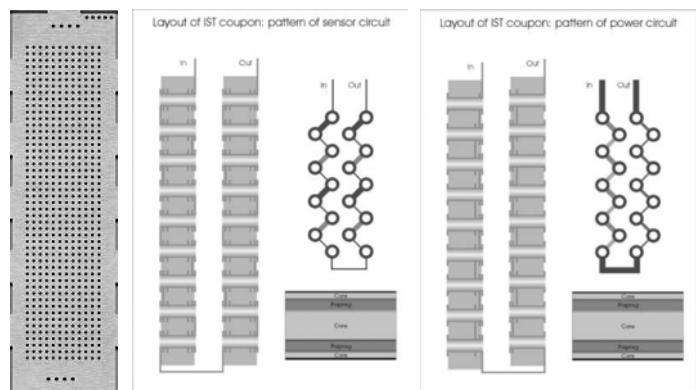


TEST VEHICLE

Daisy chain test coupons with a special design to induce ICDs in the power circuit were developed. Preliminary experiments showed that certain design aspects increase the ICD sensitivity of the test coupons. The coupons thus included the following features to maximize ICD sensitivity:

- structured innerlayers
- structured surface
- bigger hole diameter (1.0µm)
- 25 – 30 µm acidic copper thickness (with lower thickness barrel cracks usually appear first)

The following picture and diagrams show an IST test coupon:



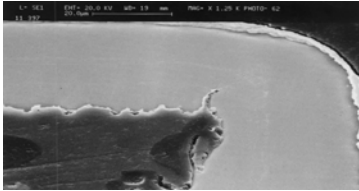
DESMEAR PROCESS

Improvements to the desmear process can only have a very marginal positive effect on the ICD performance. It is however very important to make sure that complete smear removal occurs. This is because rest smear on

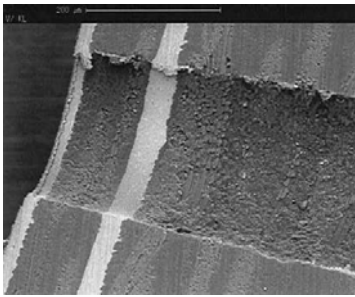
BMV capture pads and inner layer copper can lead to poor copper – copper adhesion at the affected points and subsequently to ICDs.

The following pictures show the so called K8 failure. This occurs when drill smear residue at the top of the hole is not adequately removed leading to what looks like a corner crack. This problem can be eliminated by etching with NaPS prior to desmear.

SEM image of K8 failure:



SEM Image of through hole with rest smear at top. This can lead to K8 failure if no etching occurs prior to desmear:



CONDITIONER/ETCH CLEANER

Typical conditioners currently used in the PCB industry seem to have very little effect on ICD performance.

Etch cleaning is a crucial step for interconnect reliability. This is because it roughens exposed copper surfaces thus offering more “anchorage” points for the electroless copper resulting in better adhesion.

Etching with sodium persulfate seems to have a more positive effect than using H₂O₂/H₂SO₄. Some experiments and customer experiences seem to suggest that the most positive effect results from using special etching agents such as Securiganth C (Atotech Product). However the results are inconclusive and further investigation is required.

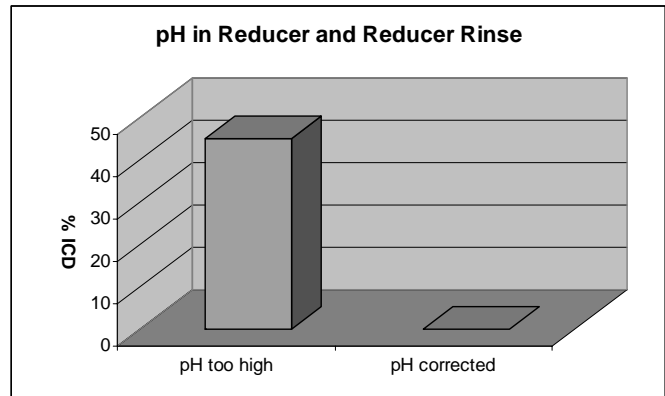
ACTIVATOR

The generally held view in the PCB industry seems to be that acidic activation (PTC) is better with respect to ICD performance than alkaline activation (ionic). In stark contrast to this, our comparisons between acidic and ionic

activation showed no significant differences with regards to ICDs.

However, mass production experience indicates that for ionic activators the pH values in the reducer as well as in the reducer rinse are crucial and need to be tightly controlled within specified limits for enhanced copper-copper interconnection.

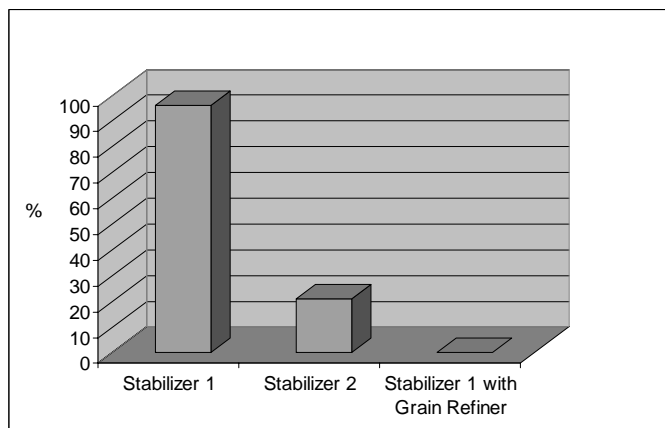
The following diagram shows the effect of pH settings in the reducer and reducer rinse on ICD occurrence for an ionic activated tartrate process:



ELECTROLESS COPPER

Exhaustive experiments were conducted to find out the effect of several chemistries and parameters within the electroless copper bath on interconnect reliability. The results showed that the stabilizer has the most pronounced effect on ICD occurrence. Changes in the type of stabilizer lead to marked differences in interconnect reliability but the best results could be achieved by addition of special grain refining components.

The following diagram shows the ICD occurrence under extreme thermal shock conditions (6x 326°C) for different stabilizer systems:



CONCLUSIONS

To be able to effectively compare the ICD performance it is important to employ the proper test methods and vehicles. TCT and IST testing can lead to seemingly random results if improper methods are used.

With solder shock testing it is much easier to get clear results from which process comparisons are possible.

The following table summarizes the process steps, which seem to have the biggest influence on IC performance. It is therefore advisable to tightly control these parameters and processes for best copper to copper interconnection.

Process Step	Desmear	Cleaner/Etch Cleaner	Activator	Electroless Copper
Effect on IC reliability	minimal	high	high	Very high

ACKNOWLEDGEMENTS

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