Through Hole Filling Production for IC Substrates and HDI Applications

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Abstract:
Conventional filling processes normally utilise an appropriate resin to plug through holes followed by further processing with metallization and circuitization. This technique is found in the production of IC substrates for cores before application of build up layers using SAP technology as well as for some handheld devices.
Demands for further miniaturisation are increasing aspect ratio which is limiting this filling process. Not least the fact that thin materials cannot be mechanically brushed requires an alternative process.
This paper describes a through hole filling process with Cu by electroplating. It demonstrates recent progress in filling through holes and discusses its current limitations.

Introduction

Various methods to produce Cu filled through holes have been presented in the last years. The method to fill such a through hole by electroplating is in our opinion the most promising one since tools (plating infrastructure) are already available and can deliver reliable processes. Our approach has been presented already on an earlier JPCA conference but shall be repeated quickly for a better understanding.

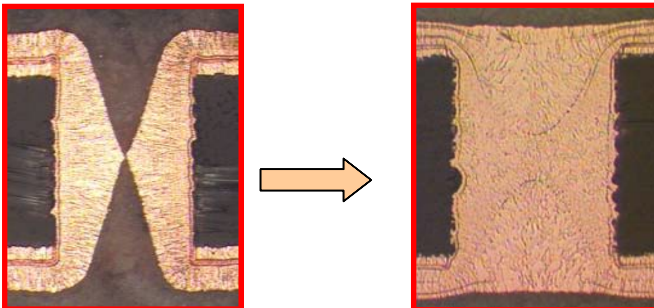

Fig. 1: Through hole filling in two steps. Left: Belly plating with RPP until merger of layers. Right: subsequent Superfilling™ of remaining Blind micro vias also with RPP

The well known horizontally conveyorized Uniplate Inpulse2 Plating system with reverse pulse plating is used in 2 steps as depicted in fig 1. In a preparatory plating step a reinforcement Cu layer is plated of a few micron (3 - 5 µm), by either a DC or a soft reverse pulse. The next step is using a very strong reverse pulse plating parameter set with which we create bumps in the middle of the through holes until they finally merge together thus leaving two blind micro vias behind. In a 2nd plating step these blind micro vias are then filled by a Superfilling™ process which is already used for BMV filling. The exaggerated belly plating is not possible with standard DC applications.
The latter is usually leading to conformal plating, in best cases to a Cu thickness of 100% compared to the surface. A merger of the conformal plated through hole would necessarily lead to a void formation in through holes (see fig 2.) DC plating leads also to a thicker Cu overplate than our reverse pulse plating with Superfilling™ technology

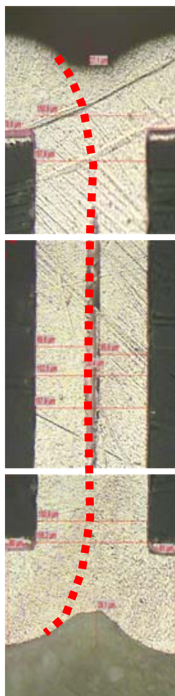

Fig. 2: Typical Through hole with void after DC Plating. The red dotted line shows the separation of the conformally plated layers. A void is resulting in the middle of the through hole.

Our Superfilling™ technology is based on an electrolyte which consists not only of Cu but also of Fe(III) which is constantly formed at the inert anodes and consumed by etching Cu either from the panel or the Cu replenishment/dissolving unit. This unique system is at the same time plating and etching. Since the Cu is in higher concentrations than Fe(III), plating dominates. Etching is primarily found on the surface and not in a via where the exchange of electrolyte is merely driven by diffusion rather than by convection (see schematic principle in Fig 3).

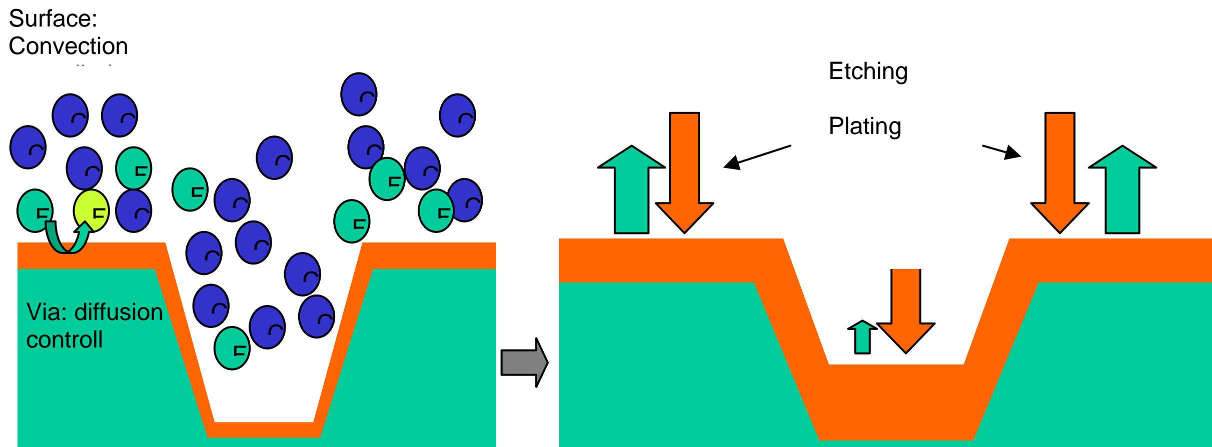

Fig. 3: Convection and diffusion controlled transport of Cu^{2+} Fe^{3+} Fe^{2+} Fe3+ is a significantly lower concentration as Cu and its transport into a via is diffusion controlled. This results in a higher etching rate on the surface than in the via or a higher net plating rate in a via.

Several investigations have proven that Fe is not co deposited in the Cu layer. In general we observed that by using the Superfilling™ process about 30 - 40 % less Cu has to be plated to achieve the filling of vias.
Applicable is this process primarily for inner layer production of chip substrates and also HDI boards.

Developments and latest results

The latest achievements are based on different areas of this process.
An online control system has been implemented to measure and control the Fe($^{3+}$) concentration by linking it to the Cu replenishment system. It allows to find the optimum in Fe3+ and further reduce the Cu overplating.
New reverse pulse parameter sets have been identified to significantly reduce the within panel variation in esp. the first plating step (belly plating).
Modification of inorganics and organics for the two different platings steps to individually improve the plating performance.
Joined projects with PCB manufacturers significantly increased the experience.

Last but not least a number of samplings led in the mean time to a more profound knowledge of process potential and limitations.

Fig. 4: shows examples in which two different boards thicknesses have been sampled.

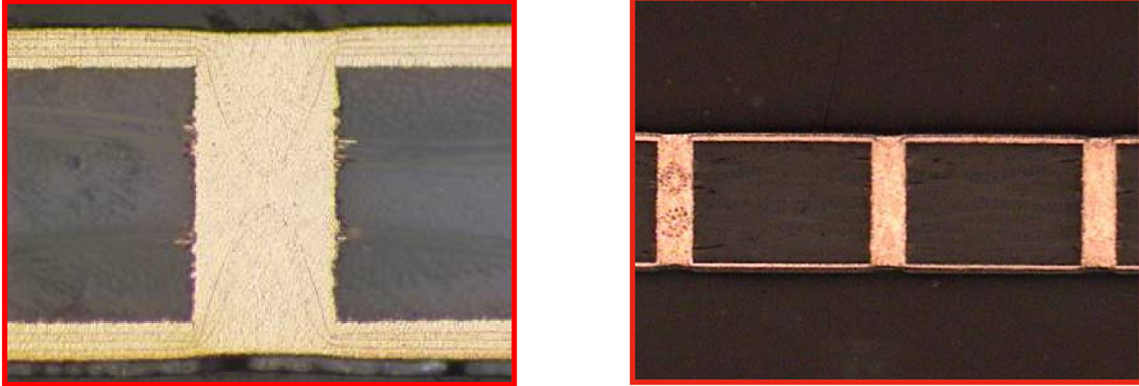

Fig 4 a. 200 µm / 120 µm Through hole plated with 23 µm Cu with 5 ASD. The remaining dimple is about 5 µm over the whole panel. Fig 4b) shows a 400 µm thick inner layer with 100 µm holes. Plating thickness is about 20 µm on a 35 µm clad, dimple < 15µm

The biggest challenge so far is the existence of densely packed through holes next to isolated ones. This affects the current density distribution so that normally a thicker Cu plating is necessary to balance a larger dimple. Due to segmented and individually controlled anodes along with a sophisticated flow management we can significantly reduce the effect of surface thickness variations to a minimum and also avoid voids in the middle of the vias

So far the process is qualified for 100 µm thick cores with 500,000 holes (100 µm) per board, a hole pitch of 250 µm! Qualification for thicker boards is ongoing and we expect to see soon 200 µm inner layers in production. The aim is to fill 400µm thick inner layers in production which are becoming kind of standard inner layer soon.

Summary

The through hole filling process is extremely advantageous since it is beneficial both from a technological and an economical point of view. It reduces the number of process step and offers further possibilities for miniaturization. The use of copper to fill through holes has significant advantages in terms of thermal conductivity and CTE match as well as the excellent inherent electrical conductivity of copper.

The process itself utilizes standard horizontal RPP panel plating equipment. It has been qualified for production, is used in small volume manufacture and will be used for high volume manufacture in 2nd half of 2008. This rather new process has been brought into a more mature phase considering the differences in layout as numbers and sizes of through holes per panel, pitch, thickness of boards etc. Current limitations (Feb 2008) are: Board thickness up to 200 µm, with 150 µm holes plated in 60 min with 35 µm Cu. It can be expected that the current limitations will fall quickly and thicker inner layers as 400 µm will be produced by this technique.