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Copper Electroplating Process for next Generation core Through-Via Filling

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ABSTRACT

The manufacturing process for substrate cores requires production of a planar surface which is subsequently used as the starting point for the high-density build-up layers. The core may be of varying thickness and is normally mechanically drilled to produce the required through-via connections which are then metalized and plugged with a thermally cured resin material. There is a current tendency for reduced core thickness and this has implications for yield, quality and ultimately for cost for product from the complete process. The plugging process itself is relatively labor-intensive and requires, as part of the sequence, a mechanical abrading or brushing process after resin cure, which can cause problems of dimensional stability, particularly for substrate cores less than 100 µm thick. The plugging resin itself has disadvantages in that it is a high-solid content material, which has a different coefficient of thermal expansion (CTE) to that of the surrounding material, including the copper metal in the via and also to that of the dielectric of the core itself, typically a glass-reinforced resin material.

The disadvantages of the existing plugging process can be eliminated by using pure copper to produce the planar surface. For the next-generation process, copper is deposited into the through vias as an integral part of the metallization process. The drilled dielectric is made conductive and a thin layer of copper metal is deposited to give a seed layer for the copper deposition process. The through-vias are then completely filled by a modified electrolytic copper deposition process, which can be accomplished in a single, fully automatic continuous processing line.

The use of pure copper has obvious advantages in that its thermal characteristics are significantly better than any type of resin material available. This fact can give more design options to utilize the improved thermal transfer capability of vias in a substrate than are currently available. The CTE of the copper-filled core is dependant only on the copper metal and the glass-supported resin of the drilled dielectric. The copper structures in the subsequent layers may be positioned directly above the copper-filled through-vias with no reliability implications. In fact, the conductive path within the substrate may be designed to utilize the more direct and parallel connection from one side of the substrate to the other.

Use of pure copper for the filling of through vias in substrates has technical advantages inherent in the use of the copper material and also the potential of improved yields due to the simplified processing required. The improvement in processing yields can have a significant impact on the overall cost of the production for the next generation of substrates.

Keywords: Cu Electroplating, Core, CTE, Thermal vias, Flip chip, BGA.

INTRODUCTION

Via hole plugging as a process is used to produce a planar surface which enables subsequent sequential lamination for production of build up structures, the planar surface is particularly important to ensure uniform dielectric spacing between circuit layers critical for controlled impedance in high frequency applications. The standard process is to use a plugging paste which is applied by methods such as stencil printing or roller coating. On top of the plugging paste there will either be the next resin layer which may be glass reinforced, or a plated copper layer. This copper surface may be used to allow production of staggered or stacked blind micro vias which are conformally copper plated or copper filled depending on the application requirements.

Various non-conductive plugging materials are commercially available to enable the plugging of core vias, critical aspects of the material are the Tg and the CTE to ensure best possible reliability of the completed structure. In [1] a review is given of methods and critical aspects of through

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via plugging used to produce sequentially laminated substrates. For HDI technology a plugging material with a low CTE and as high a Tg as possible should be chosen. The plugging pastes typically used have close to 100% solid paste with no residual solvents, there should be no air left in the paste and after curing the material should be easy to grind and remain flat with no signs of sagging. In figure 1 a microsection of a of a glass reinforced laminate material is shown after hole plugging and curing with the usual bulge of the plugging material above the surface of the drilled copper laminate. This excess material has to be removed by mechanical brushing to produce the planar surface required before processing in metallisation processes to give the “capped” via.

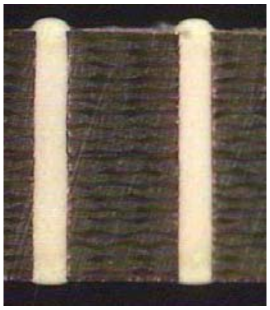

Figure 1. Substrate after plugging and curing

In figure 2 the same substrate is shown after mechanical brushing. This process is very effective at removing the excess plugging material however depending on the rigidity of the substrate this can cause problems with dimensional stability. The tendency for substrates to become thinner is making this brushing process more difficult to carry out without causing stretching and resulting in loss of registration for the following processes.

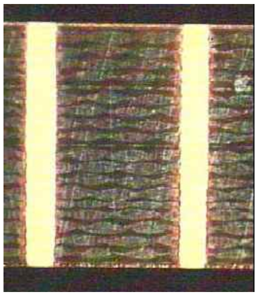

Figure 2. Substrate after brushing

Of course changes in the dimensions of the substrate can be calculated and incorporated into the design but this is another factor which can impact the overall yield of the process. As well as this the plugging, curing and brushing process has to be made in separate pieces of equipment which means that handling of work in process is increased. Figure 3 shows a microsection of a completed flip chip BGA substrate with plugged through via as a core with subsequent build up layers.

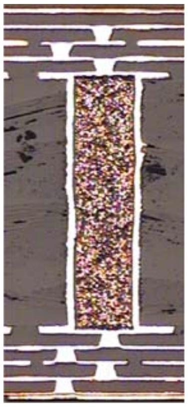

Figure 3. Plugged core in flip chip substrate

The plugged via has been metalized with electroless copper and electrolytic copper up to approx. 20 µm followed by the subsequent four build up layers each with laser drilled blind micro vias. Each build up layer is laser drilled to form the connection to the previous layer followed by the necessary thickness of copper plating to make the conductive tracks. This example illustrates well the technique of blind micro via filling to ensure void free sequential lamination. The build up layer directly above the plugged via in this example has been made with the blind micro vias positioned directly centralized on the core. This positioning will save space in the substrate design but it is not always the most reliable due to the CTE of the completed composite. Figure 4 shows a common design for positioning of blind micro vias to gain reliability for the substrate.

Figure 4. Build up layers on flip chip substrate

The filled blind micro vias have been positioned at the edge of the plugged and capped through via, this design will use more space but avoids the area of highest CTE in comparison to the remainder of the composite.

Plugged Via Reliability

In [2] the reliability of substrates with resin plugged through vias incorporating blind micro vias positioned directly on the plugged and capped through via is investigated. The paper describes this production technique as “via on interstitial via hole” or “VONI”. The quality dependence of the substrate on the particular plugging material and on the CTE of the material is investigated. A thermal stress simulation is shown which is used to aid design to improve quality. The main failure modes of the “VONI” structure were shown to be cracks in the plated barrel of the through via and delamination of plated layers caused by excessive expansion of the plugging material under thermal cycling. The causes of the delamination were shown to be related to the chemical properties of the plugging material and the amount of residual moisture remaining in the material.

Figure 5 illustrates a further reliability aspect in the plugging of through vias. The plugging material is different to the remainder of the glass reinforced resin in this example and there are non-uniformities or possible voids between plugging resin and the following build up laminated layer.

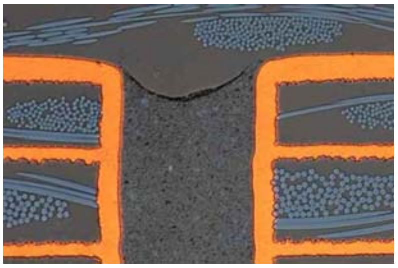

Figure 5. Plugged through via with subsequent lamination showing non-uniformity

This non-uniformity may trap moisture during the production process and be the cause of delamination and failure of the substrate.

Thermal Via Characteristics

Through vias in substrates may be designed to allow heat generated to be transferred to heat sinks on the opposite side of the material. To improve heat transfer special plugging materials have been developed to give increased performance however even the best conductive pastes do not have thermal characteristics even close to that of copper. This means that in through hole plated and plugged vias almost no heat is conducted by the plugging material in comparison to the copper barrel of the via. In [3] the design constraints to ensure effective removal of heat from electronic components are discussed. The comparison of the thermal conductivity of copper at over 300 W/m K to that of thermal pastes in the range of 0.3 W/m K to 1 W/m K is made. To overcome this problem the use of thicker copper plating or even thick copper inner layers is discussed. This use of thick copper inner layers is also used in some BGA substrates, one design shows a core with a copper layer approx 100 µm thick. An alternative is to increase the number of thermal vias but this cannot be a practical alternative where the demands for increased miniaturisation are driving all developments.

The obvious alternative to using a resin or paste type of plugging material is to plug through vias in cores with electroplated copper. Such cores are anyway processed in metallisation steps to give a seed copper layer which is then reinforced to give the final 20 µm to 25 µm thick layer so a thicker copper deposit to completely fill the via requires no great leap of imagination to consider. The problem however has been to develop a suitable electroplating process which will fill a via with a relatively small diameter and also with a high aspect ratio without requiring a thick deposit of surface copper. The process should also be capable of volume production which generally implies high current densities which are not normally possible to use for plating high aspect ratio structures.

BLIND MICRO VIA AND TRENCH FILLING WITH ELECTROLYTIC COPPER

A novel electrolytic copper plating process for blind micro via filling was described in [4]. The process has been developed for use in a horizontal plating line utilising insoluble anodes and reverse pulse plating to deposit extremely uniform copper layers. The equipment may be combined also with a horizontal pre-treatment line to give a combined electroless copper and electrolytic copper production plating system. This combination gives the advantages of a wet to wet continuous processing which ensures reliable copper deposition. As is described the use of insoluble anodes gives the advantages of uniform deposition of copper over the entire cathode area. Accurately defined pulse plating parameters may be set up due to the use of individually controlled rectifiers for each anode segment. The choice of the pulse plating parameters together with electrolyte settings allows the deposition of copper and also the etching of copper simultaneously during the plating cycle. This combination allows the filling of structures on a substrate with a minimum of surface plated copper. In comparison to conventional filling processes the amount of copper required can be reduced by over 40% to achieve a better filling result. Figure 6 shows an example of a copper filled blind micro via with diameter 140 µm and depth 115 µm filled with only 16 µm of surface plated copper. The residual dimple after plating is less than 10 µm.

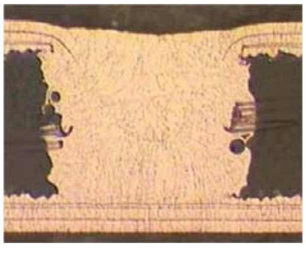

Figure 6. Blind micro via diameter 140 µm and 115 µm depth filled with 16 µm surface plated copper.

This process is currently used in full scale production in HDI applications particularly for hand held devices, figure 7 shows a microsection of stacked, filled blind micro vias and the associated attached component from such an application. The advantages of the copper filling can be clearly seen, the first filled layer provides the planar filled copper surface ideal for the following stacked, filled blind micro via. Without copper filling soldering onto the BGA would normally be expected to have significant voiding due to entrapped air. This copper filling process has in the meantime become an industry standard for the production of HDI for mobile phone applications.

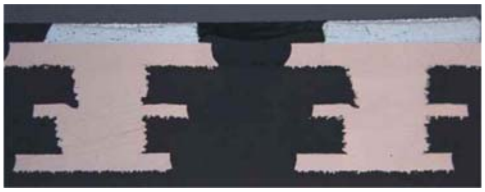

Figure 7 Filled stacked blind micro vias

The blind micro via filling technology has been further modified to enable filling of laser ablated trenches in dielectric for sub 10 µm lines and spaces as described in [4] and also in [5] and [6]. Figure 8 shows a microsection through a substrate with filled trenches showing the very uniform copper plating and also filling of the structures with low dimple. After copper plating the excess material is removed to expose the embedded tracks, this process offers a significant breakthrough in the production of substrates.

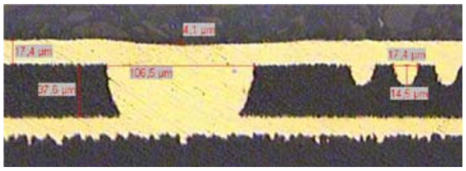

Figure 8. Laser ablated trench dimensions 106 / 37 µm copper filled with 4 µm dimple

THROUGH HOLE FILLING WITH ELECTROLYTIC COPPER

In the development work for the blind micro via filling process “Superfilling” and also for the trench filling process it was seen in early experiments that through vias were excessively plated at the centre of the hole. This result is normal when reverse pulse plating is used however the extent of the plating thickness in the hole centre was a surprise, as can be seen in figure 9.

Figure 9. Exaggerated copper plating in through via

The deposit in figure 9 is not optimal for HDI applications. There is a strongly orientated structure and the surface plated copper thickness required to achieve the result is relatively high. Extensive development work has been carried out to optimise this process and to allow filling of through holes with a minimum of surface plated copper. This factor is critical as the plating process in the horizontal equipment is generally made in the “panel” plate mode of operation. In this the entire surface of the cathode is copper plated and the resulting deposit must be circuitised by a subsequent etching step. The etching process capability is very strongly dependant on the amount of copper which has to be etched. A thick copper deposit may only be processed to give relatively coarse track dimensions, a thinner deposit allows a fine line circuit image after etching. Figure 10 shows a through via filled substrate however requiring 50µm of plated surface copper to achieve this result.

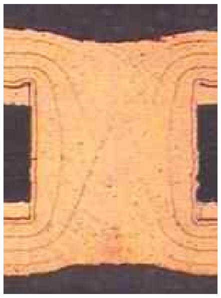

Figure 10. Filled through hole with 50 µm copper plating

As a general rule a panel plated copper thickness of 50 µm can only be etched to give structures with a dimension in the order of 100 µm. Together with the laminate copper foil this result in figure 10 is therefore not acceptable for HDI applications. There is the possibility to reduce plated copper thickness by etching or even mechanically abrading to reach the thickness tolerances for HDI however this option was discarded during development as any copper removal process adds processing steps, wastes raw material and also adds cost. Optimisation was carried out on both equipment and plating electrolyte parameters with the target to fill through vias with minimum surface plated copper and in a continuous plating line. Figure 11 shows a filled through via with only 13 µm of surface plated copper.

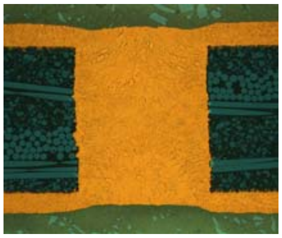

Figure 11. Filled through hole 120 µm thick, 100 µm diameter with total surface plated copper 13 µm.

The impact of rectifier modifications can be illustrated in figure 12a and 12 b

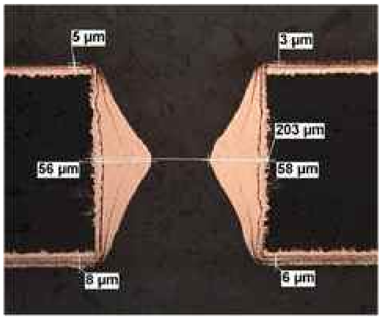

Figure 12a.

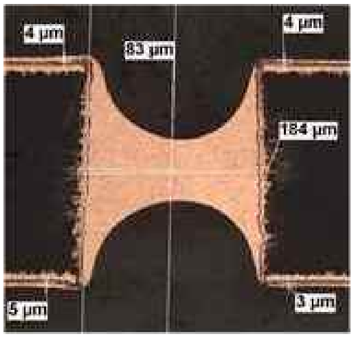

Figure 12b.

Figure 12 shows two filling tests on a 200 µm thick substrate with 200 µm diameter vias. In both cases approx. 5 µm of copper was deposited on the surface of the cathode, the electrolyte parameters were the same in both cases. The significant difference in plating result is due to the adjusted rectifier plating parameters for the experiment result as shown in figure 12b. This optimization was made possible by the use of insoluble anodes each anode with individually controlled and monitored rectifier to ensure the correct pulse wave form reaches the cathode at the correct timing. The electrolyte setting in the experiments shown in figure 12 were the same in both cases, the electrolyte is modified for filling with a specially developed additive system to withstand the aggressive pulse plating whilst maintaining uniform copper plating. The key inorganic parameters used were as follows, Cu^{2+} 71g/l, H_2SO_4 84g/l. As can be seen this high copper concentration in relation to a very low sulphuric acid concentration is not usual for copper plating however this setting was found to give best results. The plating parameters can be summarised in the table below.

Table 1. Pulse plating parameters for via filling

Forward A/dm²	Reverse A/dm²	Forward time	Reverse time
5 A/dm²	40 A/dm²	80 ms	4 ms

As can be seen the plating parameters are adjusted with a high reverse charge leading to an aggressive pulse plating deposition of copper.

Process Advantages

The CTE of copper is approx. 17 ppm/K and the CTE of typical FR4 base material varies depending on specification but is approx. 110 ppm/K. The CTE of plugging pastes varies also depending on particular type but is also in the range of that of base material at around 100 ppm/K. Figure 13 shows as a schematic the impact of the CTE on a copper plated barrel. The red arrows represent the expansion of resin base material and also plugging paste whilst the blue arrows represent the expansion of the copper plating.

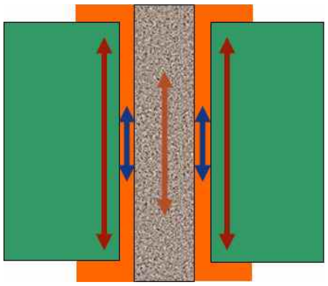

Figure 13a. Schematic of CTE stress on resin plugged through via

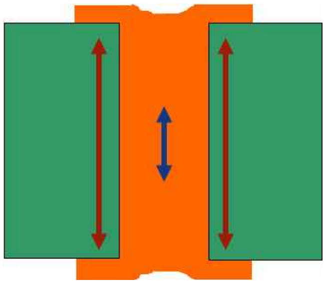

Figure 13b. Schematic of CTE stress on copper filled through via

Due to the large difference in CTE between copper and resin materials the copper in the through hole plated barrel in figure 13a will be placed under stress from both within the barrel and also from the base material surrounding the barrel. In comparison to the copper filled barrel the expansion stress comes solely from the surrounding base material. This demonstrates the increased stress due to the CTE mismatch of the plugged composite and in contrast the much reduced stress on the copper filled barrel. Due to this reduced CTE mismatch the reliability of a copper filled structure can be expected to be excellent. As an example of the reliability of a copper filled via the result in figure 13 shows the microsection of the via after 1000 cycles thermo cycle test

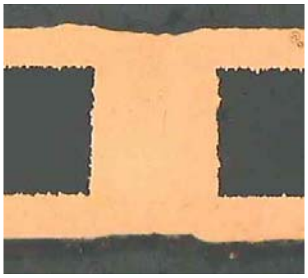

Figure 14. Copper filled core after TCT 1000 cycles -65°C to + 150°C.

Copper has obvious advantages for thermal vias due to its high thermal conductivity, this is at 360 W/m K much higher than that of plugging materials which are approx. 1 W/m K depending on specification. Table 2 compares the heat transfer capabilities as thermal resistance of through hole plated and plugged vias with a copper filled through via. This theoretical calculation was made based on a via diameter 120µm and panel thickness 150 µm.

Table 2. Comparison of heat transfer capabilities

Through via 20 µm copper	Through via 30 µm copper	Through via 20 µm copper plugged	Through via copper filled
84 K/W	62 K/W	80 K/W	47 K/W

The formula used to calculate the thermal resistance “R_{th}” was as follows,

$$R_{th} = d[\mu m] / (\lambda\ [W/mK].A[m^2]$$

In the formula „d” is the length of the heat conductor, in this case the thickness of the substrate and λ is the thermal conductivity of in this case either copper or the plugging material. A is the cross sectional area of the heat conductor, the plated copper in the barrel of the hole or the plugging material. The theoretical calculation shows that the thermal characteristics of a plated through hole are determined mostly by the plated copper thickness in the barrel of the hole. To improve the thermal performance it is more effective to increase the plated copper thickness than to use a plugging material. The best result from the theoretical calculation was found, as could be expected by simulating a fully copper filled barrel.

Also due to the increased thermal and electrical characteristics of a solid copper core the number of thermal vias required may be reduced whist maintaining an equivalent thermal capability. This again can free up surface which could be required for circuitry so allowing further miniaturization. Build up layers may be positioned directly above the filled core with no loss in reliability and this design gives the shortest and most direct circuit path from one side of a substrate to the other. An example of a substrate utilizing through via copper filling followed by sequential lamination and copper filling is shown in figure 14.

Figure 16. Core filled with electrolytic copper followed by filled BMV with minimum surface plated copper.

A further advantage of copper through via filling is that the filled copper core can be fabricated with a reduced diameter annular ring, circuit connection to the copper barrel is assured due to the solid copper connection through the substrate. This can be illustrated by the schematic of annular ring and track in figure 15.

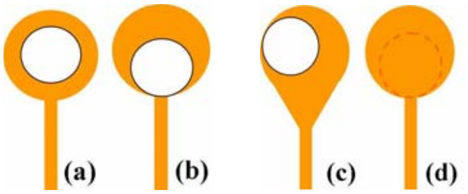

Figure 15. Annular ring design issues.

The optimum for annular ring and track is shown in 15a) where registration is perfectly centered. However the problem of poor registration and consequential connection weakness is shown in. 5b), at the connection of the track to the annular ring there is a strong possibility of break in connection especially during thermal stress during assembly. In 15c) a standard method to overcome any connection weakness is shown, the annular ring is extended to give a “teardrop” with a larger copper area. This connection is more reliable but it requires more space. With copper filled through vias as shown in 15d) the connection to the barrel of the hole is complete even when the registration is not perfect, the position of the filled barrel is given by the circular marking. The copper filled through hole can give the possibility to reduce the size of the annular ring whilst maintaining connection integrity and so making more space available for tighter spacing of circuit tracks.

CONCLUSION

The filling of through vias in substrates to enable subsequent sequential lamination is an integral part of the current HDI manufacturing process. Production methods using conductive pastes with fillers such as ceramic materials are common to produce the planar surface but have a number of disadvantages not least that increasing miniaturization makes it more difficult and time consuming for reliable production. Pure copper is the obvious material for filling of through vias to give a more reliable substrate. The process described offers a method of production of copper filled through vias which can give a more efficient thermal and electrical conductive path in the substrate. The process can also allow potentially smaller vias with equivalent thermal characteristics which could release space on the substrate for active circuit pathways. Also the production process for copper filled through vias is significantly shorter and less labor intensive.

FUTURE WORK

In [7] a simulation of the thermal characteristics of various multilayer circuit composites is described and has been used to produce an effective material model. This material model was compared to practical tests of various substrates and is intended to support design engineering of multilayer materials. Currently the use of copper filled through vias has not been tested with this method but future development work is planned to make use of the methods described.

The target for the development work is to optimise the electrolytic copper plating process to allow reliable filling of thicker substrates with higher aspect ratio through vias and with a minimum of surface plated copper. Currently in the development project a 0.4 mm substrate with 100 µm diameter via can be filled with only 19 µm of surface plated copper, this result is illustrated in figure 15.

Figure 17. Copper filled via thickness 0.4 mm diameter 100 µm. Surface plated copper 19 µm, laminate copper foil 35 µm.

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