Super High Density Two Metal Layer Ultra-Thin Organic Substrates for Next Generation System-On-Package (SOP), SIP and Ultra-Fine Pitch Flip-Chip Packages

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ABSTRACT

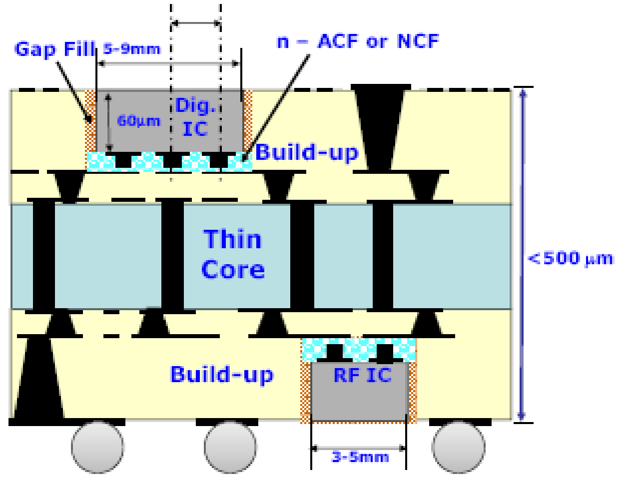
In the past decade, mobile devices have supplanted computing applications as the primary drivers for package interconnection and wiring density. This shift to low-cost consumer products has resulted in the need for miniaturized, extremely low-profile and low-cost package substrates. The current leading-edge organic package substrates for portable device SiP and multi-component packages are based on 1+2+1 build-up construction on thin cores. The latest mobile product packaging roadmaps forecast a reduction in I/O peripheral pitch from 50 – 60 µm to 20 – 30 µm and I/O count per die increasing to more than 1000 within the next two to three years. Increasing adoption of embedded active and passive component solutions is adding to the wiring demand in the substrate. However, the increasing cost of high-density organic package substrates is a major concern for semiconductor, module and system companies.

The System-On-Package (SOP) concept, pioneered by Georgia Tech PRC, is focused on convergence of functions (digital, RF, optoelectronics, MEMS, etc) in a single package or module. Some of these fundamental packaging concepts have been implemented recently in an on-going, multi-year R&D program focused on embedded thin-film passive and active components (EMAP) for mobile product applications. This project is being jointly supported by semiconductor, systems and supply chain companies. A key technology building block in the EMAP research involves ultra-thin and low-loss organic substrates with an emphasis on minimizing cost. The research targets for this substrate are 50 - 100µm thick glass-reinforced laminate cores, 15 - 20µm thick build-up dry-film dielectric, 30 - 50µm diameter through-vias in the core, 25 - 40µm diameter blind microvias, and 15 µm lines / spaces on both the core and build-up layers. The substrate is designed to match 30 µm on-chip I/O pad pitch in a peripheral configuration with two chip sizes of 3 mm x 3 mm and 7 mm x 7 mm.

This paper describes results from collaborative research to achieve the wiring density of the 1+2+1 substrate within a two metal layer (2ML) thin core with filled through vias and ultra-fine lines. The reduction in layer count and elimination of build-up layer processing is anticipated to significantly reduce the substrate cost, thus enabling the organic substrate to be competitive with re-distribution layers used in wafer-level packaging. This research includes use of a state-of-the-art electroless and electrolytic copper plating process to achieve the required ultra fine line circuitry and through-via filling. These processes have been optimized on next-generation dielectrics characterized by ultra-low loss, low dielectric constant, low CTE and low moisture uptake with stable properties up to 40GHz. Results from various processes needed to achieve the super high-density 2ML substrate will be presented, as well as reliability evaluations of the completed substrate structures.

INTRODUCTION

The focus of the EMAP consortium is the R&D of next generation mixed signal modules with embedded active and passive components to further miniaturize (thickness and form factor reduction) current SiP (System in Package) modules. The major emphasis of the EMAP consortium is on mobile product applications with focus on RF/wireless modules/packaging, and baseband processor packaging for cellular, WLAN, WiMAX and other wireless communication systems. One of the primary research projects addresses the issue of reducing the layer count and thickness, and improving the high frequency performance of the package substrate. This paper presents the latest results on process challenges, targets achieved and reliability test data from ultra-thin and low loss organic laminate substrates.



* Patent Pending

Figure 1 Embedded Active and Passive Module (EMAP) Cross-section Schematic

Figure 1 illustrates the EMAP phase 1 module cross-section using a novel “chip-last” IC embedding process technology. Detailed results from the precision cavity based embedded IC process and design have been previously reported [1,2]

Next Generation Low Loss Laminate for RF/Digital Modules in High Frequency Applications

For mobile product packaging, the key technology trends that impact the choice of substrate materials are listed below.

1. Move to higher temperature assembly processes due to elimination of lead for environmental benefits.
2. Higher frequency and higher speed of electronics systems and emphasis on RF-digital mixed signal packaging with the advent of multi-communication devices with voice, video, and internet.
3. Accelerating demand for converting wire bond ICs to flip-chip and embedded die assembly methods without the need for wafer level RDL.
4. The growing emphasis on cost reduction of substrates and packages as a significant technology driver.

These system drivers translate to organic core substrate and dielectric material needs as follows:

1. Electrical Properties: Low loss tangent and low dielectric constant for signal integrity at Gbps data rates and 1-80GHz RF performance. A major need is for stable electrical properties with varying frequency, temperature and humidity conditions
2. Thermo-mechanical properties: Low CTE to achieve high reliability for fine pitch interconnects. High temperature stability (at 260C) and low moisture uptake for reliable flip-chip interconnect.
3. Processability: Compatibility with high throughput through via drilling processes and standard plating based metallization. Low lamination temperatures below 200°C for prepregs.
4. Environmental: Pass all required fire retardant standards without the use of halogens.

The integration of embedded RF passive components in the EMAP substrate places an added requirement for stable low loss dielectrics. The dielectric material used in the current EMAP substrate consists of two distinct low loss thermosetting polymers; (a) a thin core glass reinforced laminate (RXP-1) and (b) a thin dry film build up dielectric (RXP-4). The research results reported in this paper are restricted to the RXP-1 core with two metal layers interconnected by copper filled through vias. The build-up microvia substrate results will be reported in the future. The RXP-1 core is a glass fiber reinforced organic laminate with thickness in the range of 50-125µm. The RXP-1 has stable dielectric constant of 3.25 and loss tangent of 0.004 at 1-20GHz as shown in Figure 2. In addition, RXP-1B laminate has a medium CTE (10-13ppm/C) which is critical for improved fine pitch interconnect reliability at the first and second levels. Another benefit of the RXP-1 system is its high Tg (~300C) above the lead-free reflow temperature of 260C, which leads to excellent thermal stability during assembly processes. The lamination temperature of the RXP-1 prepreg is around 177C and halogen-free versions of the laminate system are under development.

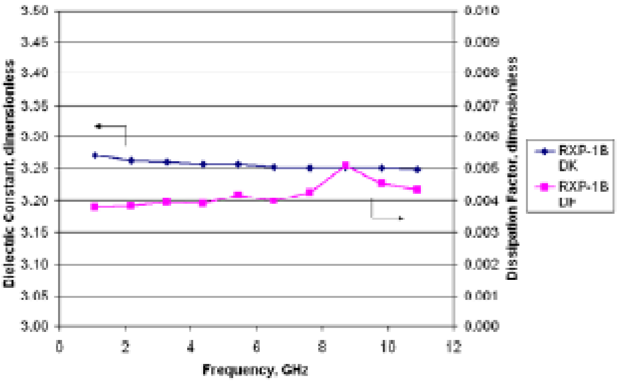


Figure 2 Measured Dielectric Constant and Loss Tangent for RXP-1 Thin Low Loss Laminate

A comparison of RXP-1 storage modulus against BT laminate (HL832HS) is shown in Figure 3. A modulus drop can be seen for BT above 200C, whereas the RXP-1 modulus is stable and predictable.

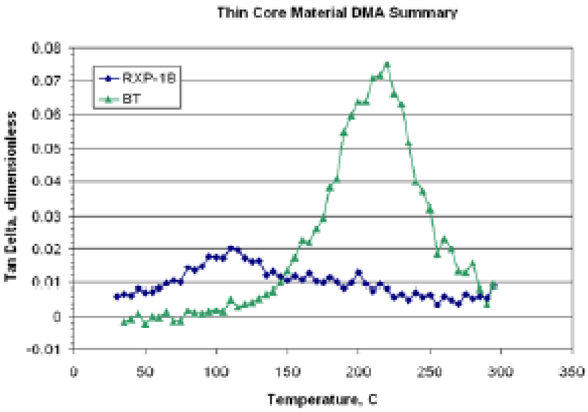


Figure 3 Thermal Stability Comparison for RXP-1 and BT Thin Core Laminates

Fine Pitch Routing Design Rules and Test Vehicle

The substrate design rules include a minimum copper line width and space of 15 µm, blind microvia diameter of 25 µm and through hole diameter of 50 µm. Line width and space of 10 µm and through hole diameter of 30 µm was also designed for testing the process limits. Line widths below 15 µm were targeted for semi-additive process (SAP) and lower cost subtractive etching was used for >15 µm lines. The top view of the two metal layer structures and details of three types of microvia daisy chains are shown in Figure 4. The “BV” structures include only blind microvias in the build-up layer, and the “MSTK” structures include both blind microvias and through vias in the thin core. The daisy chain structures used in this study are the “THRU” which consist of 250 through vias stitched together and terminated using ten blind microvia to allow for probing each of ten segments in the daisy chain on the top surface of the 1+2+1 EMAP substrate as shown in the cross-section at the bottom of Figure 4.

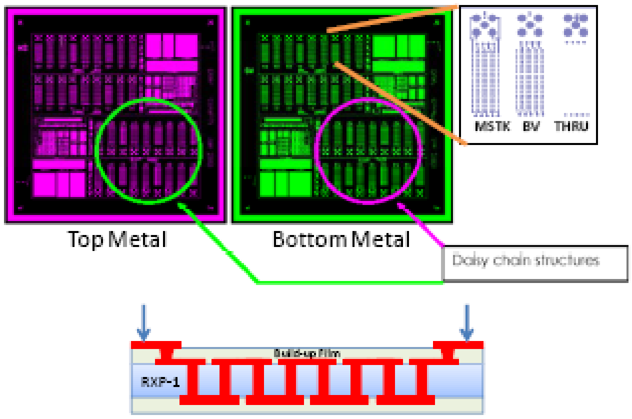


Figure 4 Ultra-Thin Substrate Process Test Vehicle for Via Reliability and Fine Line Patterning.

Photo-masks were fabricated using low cost emulsion printed on Mylar film. The limiting resolution of the emulsion (printed at 20000 dpi) was approximately 12 µm and was used in contact lithography mode using a collimated broad spectrum Hg-arc lamp source. Figure 5 shows a process flow of the test vehicle fabrication process used for this evaluation using RXP-1 laminate of 115 µm thickness and 18 µm copper foil cladding.

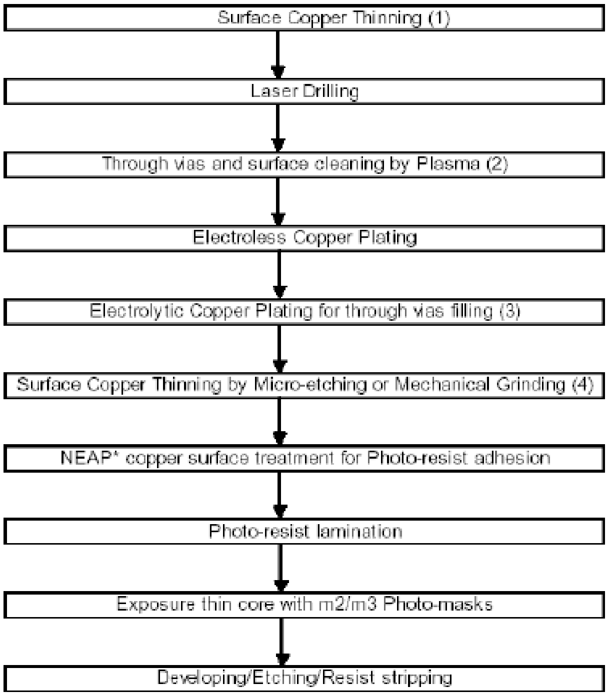


Figure 5 Process Flow for Super High Density Two Metal Layer (2ML) Thin Core Substrate with Copper Filled Through Vias

The first copper thinning step was done using CuCl2 spray etching with a target thickness of 8 µm +/- 2 µm. The copper thinning increases UV laser drilling throughput by reducing the thickness of ablated copper.

Through Via Drilling and Desmear Process Challenges

Figure 6 illustrates the available technology options for creating ultra-small and fine pitch through vias in organic laminate thin cores.

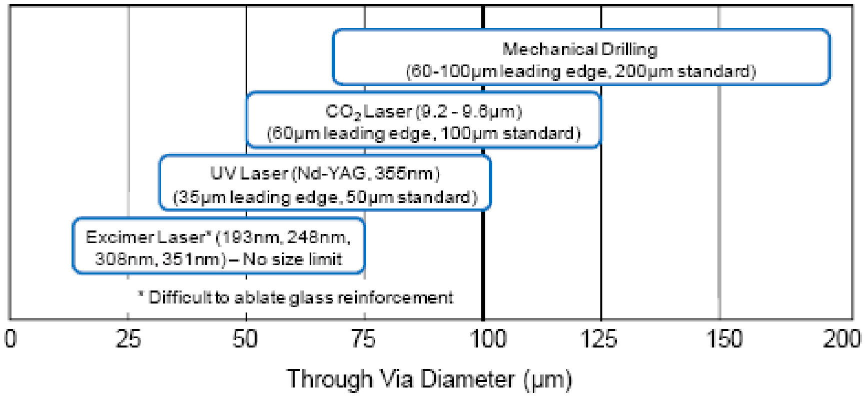


Figure 6 Mechanical and Laser Drilling Technology Options for Ultra-fine Pitch Through Vias in Organic Cores

For the targets of 30 -50 µm diameter, UV laser ablation was chosen as the front-up approach. The three major laser ablation options and their associated via size and density are shown in Figure 7.

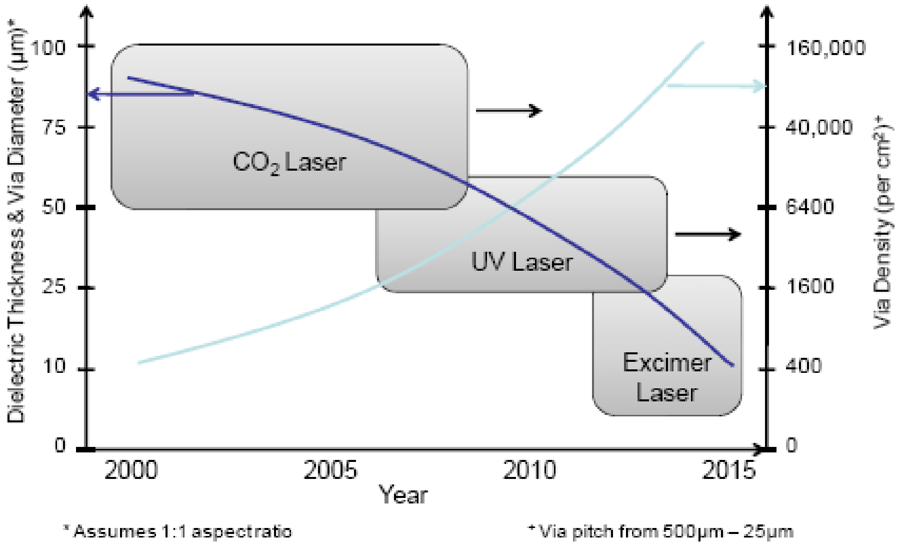


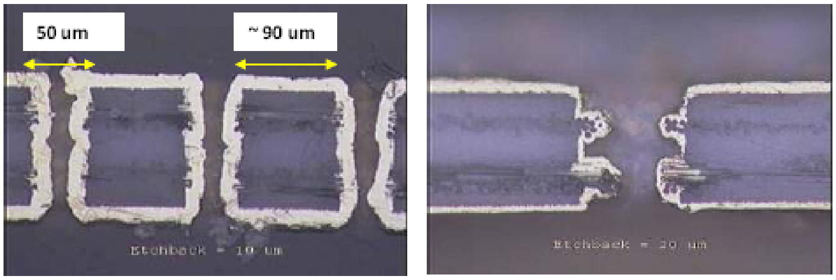
Figure 7 Comparison of Via Density Capability of Laser Ablation Processes

The through vias were designed for 50 µm diameter at 125 – 150 µm pitch, 40 µm diameter at 100 – 125 µm pitch, and 25 – 30 µm diameter at 75 – 100 µm pitch. An ESI 5210 Nd-YAG laser operating at 355 nm was used for the through via ablation and the results are shown in Figure 8.

(a) 25µm Diameter/ 75µm Pitch
(b) 40µm Diameter/ 100µm Pitch
(c) 50µm Diameter/ 125µm Pitch

Figure 8 Ultra-fine Pitch Through Vias in RXP-1 by UV Laser Ablation

One of the major challenges in moving to very small through via diameters is the control of the desmear process. In conventional substrate technology, the typical etch back of the resin during desmear can be as high as 25 µm, which is equivalent to the via diameter targets in this research. An optimized plasma desmear process was developed for RXP-1 using a PlasmaEtch BT-1 system operating at 13.56MHz and 300-500W RF power. Since current chemical desmear processes have been designed for etching epoxy based polymer dielectrics, they were ineffective for the advanced non-epoxy resin system used in RXP-1. Figure 9 illustrates the microsections of 50 µm through vias after optimized desmear process (left) and over-aggressive plasma etch cycle (right) indicating the tight process control required for fine pitch through via metallization.



(a) Optimized Plasma Desmear (b) Overetch During Plasma Desmear

Figure 9 Plasma Desmear Process Results on RXP-1 after electroless copper metallization

Through Via Filling Process by Copper Electroplating

A key to achieving highest component density and I/O density for ultra-thin single and multi-die packages is the ability to form filled and planarized through vias to enable via-in-bond pad designs. Conventional paste filled via techniques face severe barriers when the through via diameter scales down to below 50 µm due to the difficulty in pushing the particulate filled polymer pastes into the conformal copper plated vias. Hence, a copper filled through via method was explored and demonstrated for the sub-50 µm diameter through vias. Traditional DC plating process was initially used for via filling, and the results are shown in Figure 10. The limitation of this process was the excess copper thickness build-up on the top and bottom surface resulting in a final thickness on the surface of ~35 µm, which reduces the throughput of the copper thinning required prior to lithography and patterning.

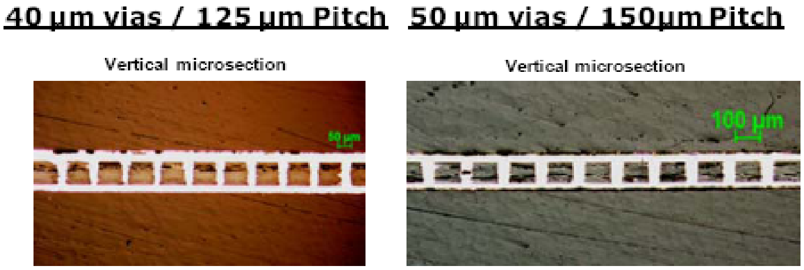


Figure 10 Microsections of 40 and 50µm Through Vias Filled by DC Copper Plating

To address this problem, a novel super-filling process technology based on the Inplate DI system has been demonstrated as shown in Figure 11. This process uses a proprietary set of additives to control the plating distribution within and outside the through via. An aggressive roadmap has reduced the surface plated copper thickness for 100 µm diameter through via filling from 50 µm in 2005 to 10 – 13 µm in 2008.

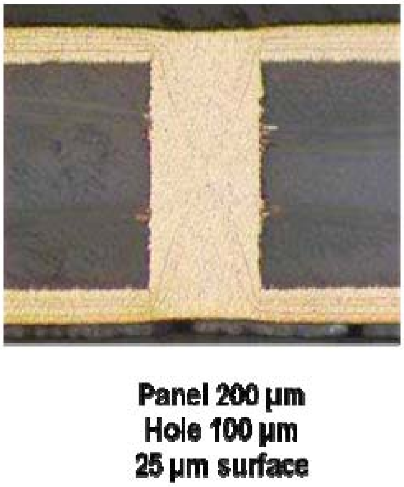


Figure 11 Cross-section of Copper Filled Via Showing Minimum Dimpling on the Surface

The copper filled through vias using this super-filling process have passed up to 1000 cycles air to air TCT testing at – 65°C to + 150°C with no failures.

Surface Copper Thickness Control and Fine Line Patterning

For low cost two metal layer high density substrates, a subtractive etch process for patterning the copper layers is preferred over SAP process. The target copper thickness for the two metal layers was 8 – 10 µm to allow for sub-25 µm line / space etching. An additional chemical etch based copper thinning process was implemented after the through hole filling. Since the through vias are filled with solid copper, no concerns of via etch-out exist during chemical copper thinning. An optimized thinning process was demonstrated with a final thickness on both sides of the RXP-1 core of 10 µm.

Line and space (L/S) resolution is also related to the photoresist resolution and film thickness. In general, the minimum L/S that can consistently be formed using low-cost photoresists in a production environment is approximately one to two times that of the resist thickness. The high-performance dry film photoresist used in the investigations was 15 µm (0.6 mil) thick. Therefore, the finest circuit traces were expected to be in the range of 18µm to 22.5 µm. Figure 12 shows top view and cross-sections of 20 µm lines / spaces etched in 12 µm thick copper.

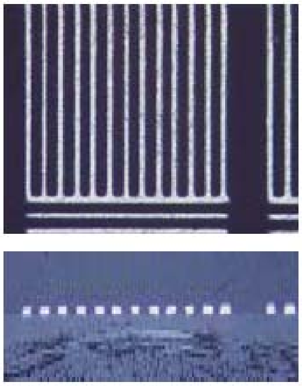


Figure 12 Subtractive etching of 20 µm lines / spaces in 12 µm thick copper

Optimization of the above process steps resulted in the demonstration of copper filled through vias of 50 µm diameter in the RXP-1 thin core as shown in the X-Ray images in Figure 13 and cross-section micrograph in Figure 14.

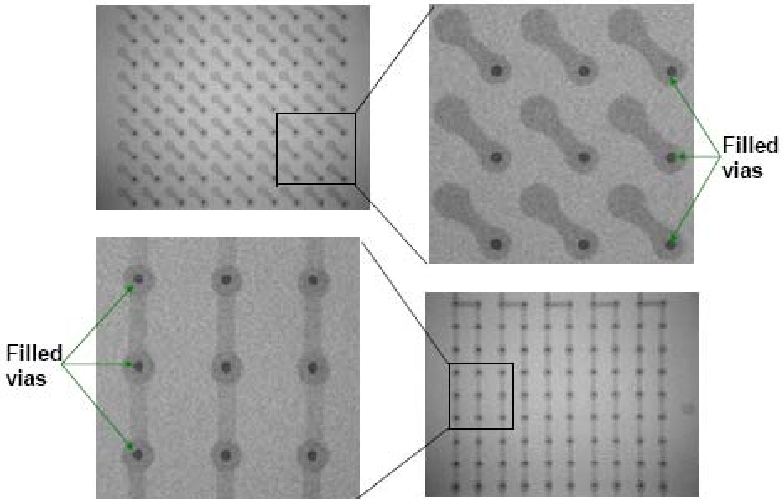


Figure 13 Top view of 100 µm pitch flip chip routing with three lines at 8.6 µm L/S (left) and four lines at 6.7 µm L/S (right) per channel

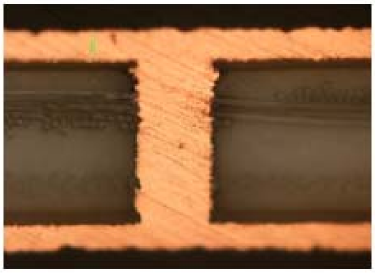


Figure 14. Cross-section micrograph of 50µm Diameter Through Vias Filled by DC Copper Electroplating in RXP-1

The finest through vias targeted were 30 µm diameter at 75 µm pitch and an X-Ray image of a via array is shown in Figure 15.

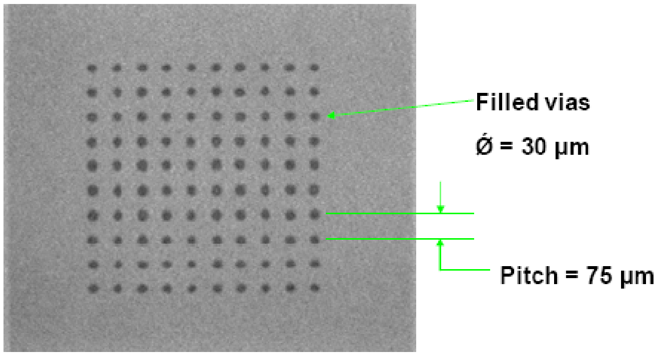


Figure 15. Array of 30 µm Diameter Filled Through Vias at 75 µm Pitch

Thermo-Mechanical Reliability Evaluation

The reliability test conditions were based on JEDEC standards and mobile product package test conditions provided by EMAP member companies. The test conditions used for the 2ML RXP-1 substrate were:

1. MSL-3 Preconditioning, JEDEC/IPC JSTD020D-01
    a. Moisture bake out at 125°C for 24 hrs
    b. Accelerated soak at 600C, 60%RH for 40 hrs
2. 3X lead-free solder reflow excursion, peak temperature 260°C.
3. Thermal shock test according to JESD22-A104C, -550C to +1250C. The cycle time was 30 minutes and the transfer time was less than 5 seconds.

The reported data was collected from four substrate panels and multiple sets of THRU daisy chains at various locations in each substrate. A sample of the resistance measurements is shown in Figure 16, including a schematic showing the nomenclature of probe pads for clarity.

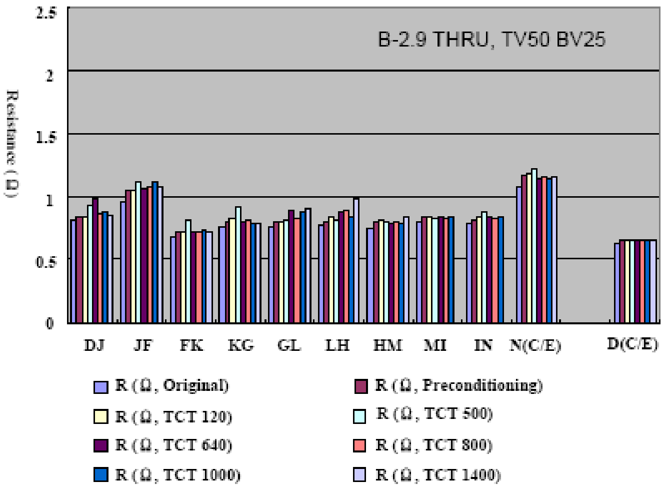


Figure 16 Daisy Chain Resistance Measurements Taken at Periodic Intervals for THRU daisy chain with 50 µm copper filled through vias and 25 µm blind microvias used for termination and probing.

Testing and statistical data analysis for the 2ML and 4ML RXP substrate is in progress, and the first ~100 THRU daisy chains tested have passed 1400 cycles with a cumulative via failure rate of 1-2%. Failure analysis by micro-sectioning was performed and in all failed THRU daisy chains, the failure was attributed to microvia cracking due to thin via wall plating from process induced defects. No copper filled through via failures have been observed to date. The reliability of the MSTK and BV daisy chains will be reported in the future.

CONCLUSIONS

The next generation of mobile product multi-die packages and SiP modules will require a combination of low profile, high interconnect density, stable GHz frequency performance and low cost. As part of the university-industry consortium on embedded actives and passives (EMAP), a novel set of process technologies have been demonstrated for copper filled through vias and fine lines on a new thermosetting low loss organic laminate RXP-1. The resulting two metal layer substrates represent some of the highest density ultra-thin substrates demonstrated. The copper filled through vias and fine lines have also passed 1000 cycles thermal cycle reliability testing without any failures.

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