Electrolytic Deposition of Fine Pitch Sn/Cu Solder Bumps for Flip Chip Packaging

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Abstract

Current methods for the formation of pre-solder bumps for flip chip attachment use stencil printing techniques with an appropriate alloy solder paste. The continuing trend towards increased miniaturization and the associated decrease in size of solder resist opening, SRO is causing production difficulties with the stencil printing process. Practical experience of production yields has shown that stencil printing will not be able to meet future requirements for solder bump pitch production below 150µm for these applications.
This paper describes latest developments in the electrolytic deposition of solder to replace the stencil printing process; results from production of 90µm bump pitch solder arrays with tin/copper alloy are given. The solder bump is produced with a specially developed electrolytic tin process which fills a photo resist defined structure on the SRO. The photoresist dimensions determine the volume of solder produced and the subsequent bump height after reflow.
Investigations on the bump reliability after reflow are shown including copper alloy concentration at 0.7% and x-ray investigation to confirm uniform metal deposition. The self centering mechanism found in the bump production process during reflow is presented and the capability to correct photoresist registration issues.
The solder bumps are shown as deposited onto an electroless nickel/gold or electroless nickel/palladium/gold final finish which serves also as a barrier layer to copper diffusion into the solder bump.
Discussion of further development work in the production of alloys of tin/copper together with silver are given with first test results.

Key words: Solder bump deposition, flip chip bump, alloy solder bump.

Introduction

The current main market driver for consumer electronics technology is in the hand held device sector and in particular can be seen in the increasing growth in the market share of Smart Phones. For this technology the target is to cram more and more intelligence onto a shrinking mother board which means more intelligence into the individual components. For all these devices one of the targets is to improve battery performance which means a larger battery volume but a reduced available space for the device mother board. To meet the reduced size available the component sizes have also to be reduced whilst at the same time offering greater capability. Critical issues are the component footprint followed by the thinness and the weight of the corresponding chip package and at the same time the requirement to bridge the increasing "IO interconnect gap". Basically the problem can be represented in the decrease in the size of silicon geometries following Moore´s Law and the slower shrink in the size of PWB technology. Aspects of this development are discussed in [1]. The standard method for component attachment for smart phone applications is using flip chip solder ball attachment. The solder ball site is defined by a photo imaged solder mask and the solder ball is produced by using screen print techniques with a suitable solder paste with specific alloy composition.

This screen printing method is now reaching its technology limits in terms of the feature size which can be reliably produced. Figure 1 shows one of the problems associated with screen printing when the ball pitch is reduced.

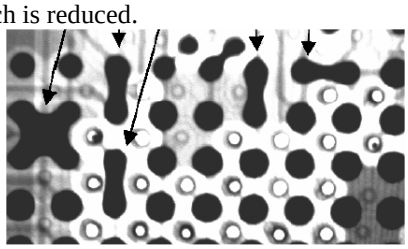


Figure1: X-Ray Analysis of Solder Ball Short After Reflow

The X-ray analysis after component attachment shows very clearly the shorts in the solder ball. A further impact on process yield is due to the reduction in the size of the stencil opening to match the size of the required solder ball to be produced. At least eight average solder particles should fit across the narrowest part of the stencil opening however the reduced size of solder particle gives a greater surface area from which oxides must be removed. The smaller size of the deposits however means that there is less flux available to remove the oxide and this can lead to solder wetting issues. At the same time small stencil openings mean reduced solder volume and it is more difficult to print solder paste at area aspect ratios below 0.8. Figure 2 shows the impact of small stencil opening and retained solder paste which will result in missing solder balls on the substrate.

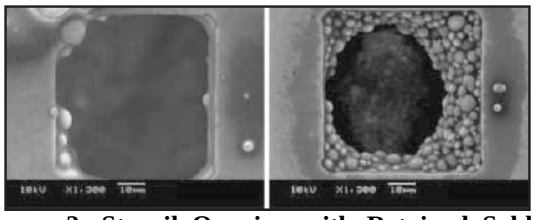


Figure 2: Stencil Opening with Retained Solder Paste

Currently the technology limit for solder paste printing is being pushed; experiments suggest that a bump pitch in the range 100µm to 130µm is the limit for state of the art production processes. Figure 3 shows a projected representation of reduction in solder resist opening (SRO) with solder resist height.

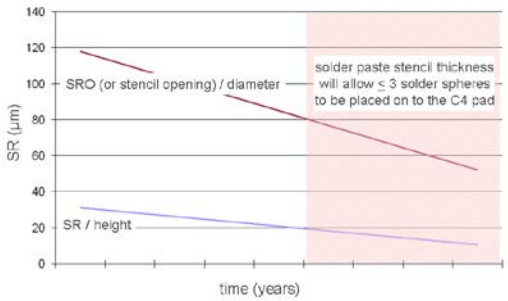


Figure 3: Technology Limit Projection for Stencil Printing

As an alternative to the standard stencil application the use of an electrolytic deposition of solder bumps has been proposed. Electrolytic processes have advantages over the stencil based process,

- Electrolytic processes are applicable for various dimensions of SRO.
- Reduced SRO and bump pitch do not restrict the deposition process.
- Imaging of the SRO can be with existing processing technology.

The basic principles in electro deposition of metals are well known in the semiconductor industry and the associated equipment may be modified for solder bump deposition. However one of the disadvantages of electrolytic processes is that alloy deposition with requirement for constant alloy concentration within tight control ranges can be difficult to achieve. Alloy concentration, the critical factor for solder ball reflow performance, is dependant on a number of factors including electrolyte concentrations which may be held constant but also plating current density which is dependant on the substrate geometry and is not always uniform. A solution to this problem using a pure tin electrolytic deposition and utilizing electroless deposits of copper and silver offer a potential solution to this problem.

Electrolytic Solder Bump Deposition

An electrolytic solder bump process should be capable of producing different structure sizes within a reasonable production time. The metal deposit must not be contaminated by any organic material and the deposit geometry after reflow should be uniform without any void or inclusion formation. Also the production process should fit into the existing infra structure of substrate manufacture as far as possible to reduce investment cost. The first developments in a production capable electrolytic bump deposition system were presented in [2]. The process uses standard photolithography to define the area for solder deposition; the plated area will determine the size of the solder ball after reflow due to the volume of solder deposited. To allow electrolytic deposition the first process step is the deposit of en electroless copper seed layer onto the prepared solder mask which has defined the SRO. The electroless copper seed layer also has a secondary role in supplying the source of the copper ions to achieve the required Sn/Cu alloy after reflow.

Figure 4 shows a micro-section through a plated pure tin solder bump with SRO pitch 90µm which has been deposited onto a copper pad prepared with electroless NiAu final finish.

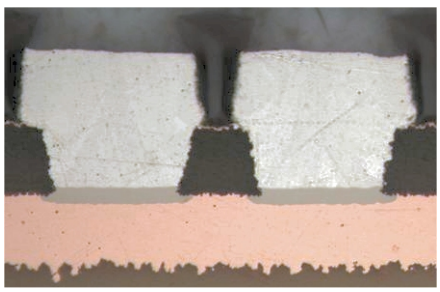


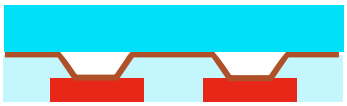
Figure 4: Pure Tin Solder Bump after Deposition

The solder deposit is produced from an electrolyte similar to standard pure tin electrolytes for electronics applications however with the addition of special additives to ensure uniform wetting and void free filling of the structures. The process sequence used is given schematically below with cross sections of the SRO to be filled.

1. SRO definition with solder mask

2. Electroless copper seed layer deposition

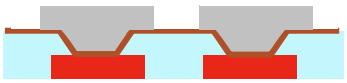
3. Plating resist lamination.



4. Plating resist exposure and development

5. Deposition of pure tin

6. Removal of plating resist



7. Removal of electroless copper seed layer

8. Reflow to form SnCu bumps by Copper diffusion of electroless seed layer

The final stage in solder bump production is the reflow process, step 8 in the process sequence above. A micro-section after reflow is shown in figure 5, the solder deposit as shown in figure 4 was reflowed to give the uniform solder ball.

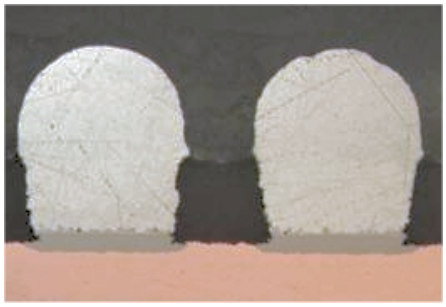


Figure 5: Solder Bump with 90µm Pitch after Reflow

The solder bump pitch is defined by the plating resist lamination process; in this case 90µm bump pitch was imaged. The process quality is determined by the registration of the plating resist and this is a critical factor in the potential yield of the electrolytic solder deposition process. Figure 6 shows a deposit on to a substrate with poor registration of the plating resist

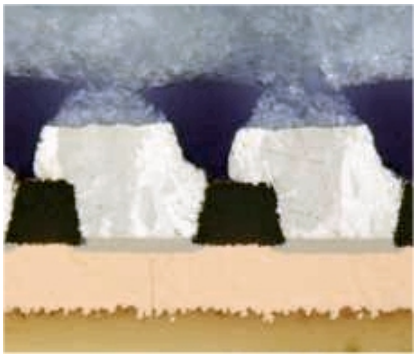


Figure 6: Solder Bump with Poor Plating Resist Registration

Despite the poor registration the solder ball formed after reflow is perfectly centered over the SRO, this is shown in figure 7. This effect is due to the self centering of the liquid solder ball during the reflow process and can correct a certain degree of plating resist miss-registration.

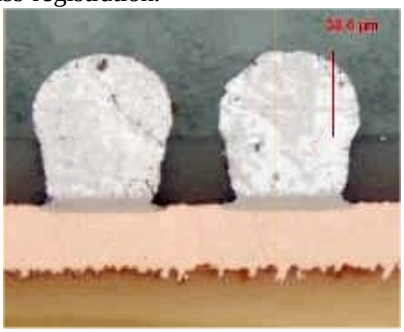


Figure 7: Solder Bump with Poor Plating Resist Registration after Reflow

To investigate the uniformity of the plated and reflowed solder bumps X-ray analysis is made. This has the advantage of showing any voiding which may be present and also to control the uniformity of the bump. Figure 8 shows a typical result of the X-ray investigation with no signs of void.

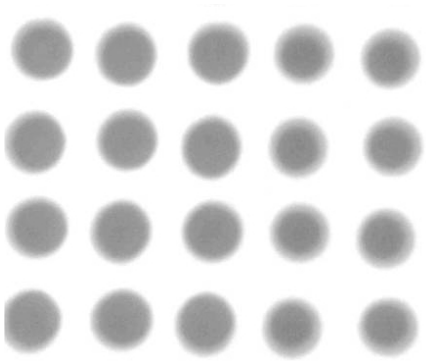


Figure 8: X-Ray Analysis of Solder Bump after Reflow

This void free uniform solder bump production has been prepared for customer qualification after process optimization.

Solder Bump Reliability

The target for the solder bump alloy in this case was a tin copper alloy with 0.7% copper. The source of the copper ions for the alloy is the electroless seed layer used to metallise the solder mask surface. Theoretical tests were made to determine the optimum electroless copper thickness with the size of the SRO to give the correct alloy content. As in this case an electroless nickel and gold final finish was used to isolate the copper substrate the only source for copper ions was the seed layer. Calculations showed that an electroless copper layer of 0.15µm to 0.2µm together with an 80µm diameter bump diameter and solder mask depth 20µm will give an alloy content of 0.7 % to 0.9 % copper by weight in the final reflowed bump. To confirm this calculation differential scanning calorimetry (DSC) investigation of the plated deposit was carried out to check the melting point of the alloy, the result is shown in figure 9.

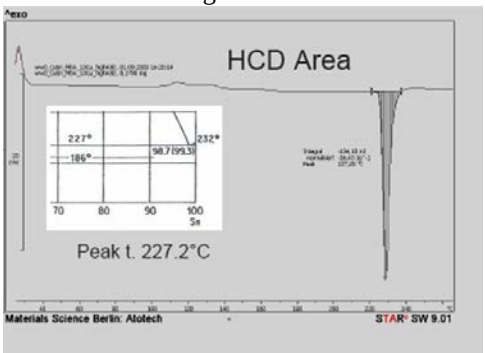


Figure 9: DSC Analysis to Confirm Alloy Content and Melting Point.

Tests on bump melting point were made in high current density deposited areas and also low current density, the tests were deliberately targeted to give a wide spread of current densities to compare the bump melting point over the complete deposit range. Due to the fact that the plating electrolyte can only deposit pure tin and the source of copper ions is an electroless process current density effects should not have any impact on alloy content. This result was confirmed by DSC and also by FIB analysis of reflowed bumps as shown in figure 10.

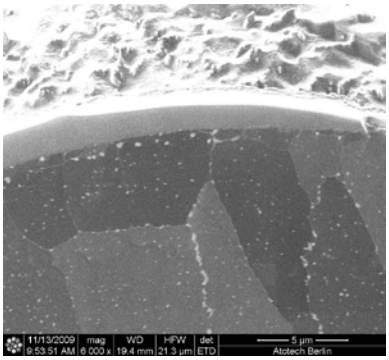


Figure 10a: FIB of Solder Bump Surface after Reflow

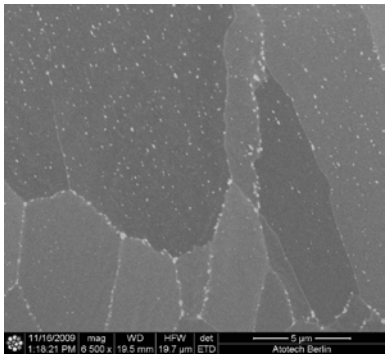


Figure 10b: FIB of Centre of Solder Bump after Reflow

Further investigations have been made on the quality of the solder joint and the interface to the surface finish, in this case electroless nickel/gold. Figure 11 shows the FIB cut through the interface before reflow

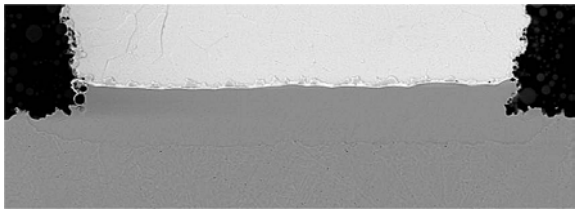


Figure 11a: FIB of Intermetallic Layer before Reflow

After reflow the FIB was repeated to show the growth in the intermetallic.

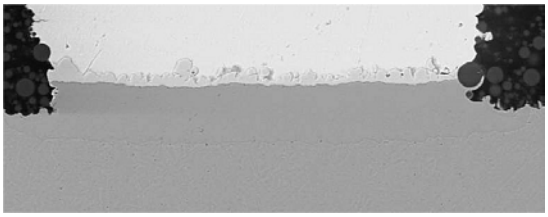


Figure 11b: SEM of Intermetallic Layer after Reflow

Solder Bump Reliability and Tin Whiskers

An important factor in the use of pure tin plated deposits is the question of tin whisker growth. To check the possibility of whisker formation tests were made with the tin plated solder bumps before any reflow process was made. Plated substrates were stored for one year to check the occurrence of whisker and thermal cycling tests were carried out. No whisker occurrence was seen after 312 h / 60°C and also after thermal cycle testing with test parameters +85° C for 10 min and -55° C also for 10 min at transfer time 10 seconds, with in total 1000 cycles tested. Figure 12 shows the surface view of the solder bumps before reflow but after 312 hours at 60°C.

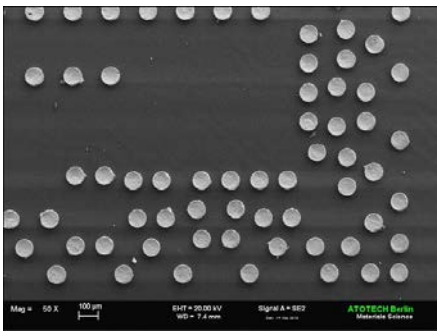


Figure 12: Solder Bumps after Thermal Exposure 312 hours at 60°C.

In all tests carried out no significant whisker formation could be found. One explanation for the good stability of the solder bump is the use of a newly developed anti-oxidant process as a post treatment for the solder bump surface. This treatment gives added benefits such as improved solderability after steam ageing and pressure cooking. The tin surface is less prone to corrosion during any temperature excursions together with high humidity. Tin discoloration is prevented also under high humidity conditions and this gives an improved contact resistance when using lead free BGA solder balls

Tin/Copper/Silver Alloy Bump Production

To achieve a low melting point solder bump with tin, copper and silver alloy a final processing of the deposited bump with an electroless deposit of silver is being investigated. Again the use of an electroless deposit overcomes the difficulties of ensuring alloy content from a plating electrolyte. Deposition of a uniform alloy of Sn/Cu/Ag and maintaining the alloy content over a wide current density range and substrate geometry range would be difficult and very costly. First tests have been made with the "Silver Cap" technology as shown in the microsection in figure 12.

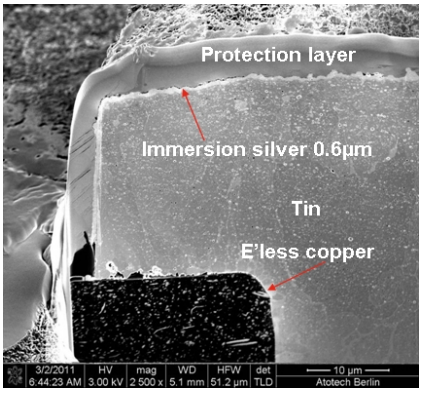


Figure 13: Solder Bump with Silver Cap.

After removal of the plating resist and the electroless copper seed layer an electroless deposition of 0.6µm of silver is made to the surface of the pure tin bump. After reflow, diffusion of both the electroless copper from the seed layer and the electroless silver from the surface combine to form the target alloy concentration. This process is in the early stages of development and further testing is being carried out.

Summary and Further Developments

The target of the initial development was a pure tin based electrolyte system capable of producing complete solder bumps on the C4 side of the IC substrate and simultaneously to produce the solder base on the BGA side. The electrolyte composition is specified to meet the lowest alpha count emission requirements and also the carbon co deposition standards. This is achieved by careful source of electrolyte raw materials and also use of an insoluble anode process in the tin deposition cell, alpha emitting isotopes in tin plating processes generally are as a result of contamination with lead. Elimination of any possible contamination of lead in anode material is critical to prevent this. The process is capable for deposition of tin alloys into all future designs and there is no restriction on SRO dimension. The production process is similar to the semi additive process (SAP) which is the standard for IC substrate production and can fit well into existing processing technology; all reliability tests have been completed.

The solder bump deposition is now being developed for use with copper post processes. For this application the defined SRO is first filled with a copper deposit from an electrolyte to plate and fill the

structure. After the copper deposition step the pure tin electrolyte is used to complete the structure as shown in figure 12.

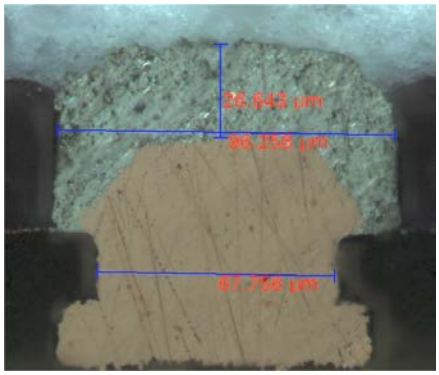


Figure 14: Copper Post with Solder Cap.

Solder Deposit for "Deep Bump" Plating using Second Organic Layer (SOL)

Development work is being made to enable production of deep solder bumps and to eliminate the use of a plating resist. The disadvantage of the plating resist is that the overall process quality and the final yield is very dependant on the registration of the imaging, figure 6 gives a clear example of the problem of miss-registration which can lead to complete failure of the solder bump formation. To eliminate the need for the plating resist imaging a second organic layer is laminated onto the substrate over the solder mask before any imaging or laser drilling is made. The laser drill process is used to form both the via in the second organic layer and also the SRO in the solder mask. In this way there is no problem of miss-registration between solder mask and the second organic layer. The substrate is then metalized in the standard way over the whole panel surface with electroless copper and finally the pure tin deposit is made to form the solder bump. This deposition is made in the "panel plate" mode of operation which means that the metal plating uniformity is better than the usual pattern plating mode. Figure 15 shows a micro-section of the deep bump plated deposit.

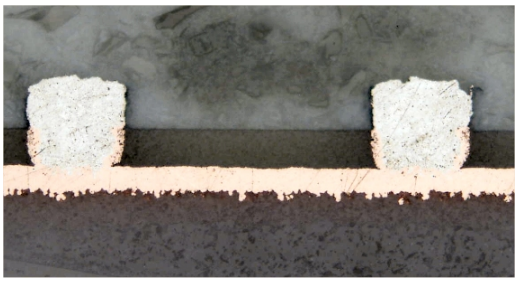


Figure 15: Deep Bump Deposit after "SOL" Removal

After metal deposition a differential etch of the whole surface is made to selectively remove metal from the panel but leaving the solder bump intact. Following removal of the second organic layer the solder bump is exposed. Initial tests with this technology have confirmed the uniformity which can be achieved in terms of solder bump distribution; current activities are concentration on optimizing the second organic layer processing to ensure optimum bump form determined by the laser drilling of the substrate.

References

[1] Bernd Appelt, "Heterogeneous Packaging: SiP based on 2.5D and 3D Integration", Proceedings of the 2011 EMPC, Brighton, UK, September 12th to 15th, 2011.

[2] Dr. Nina Dambrowsky, Frank Hilbert, Sven Lamprecht, Kai-Jens Matejat and Dr. Bernd Roelfs "The Smaller the Better - Simultaneous Electrolytic Solder Deposition on Both Sides of a Fine-Pitch Package Substrate", Proceedings of the SMTA Toronto, May 2011.