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Fabrication of High Aspect Ratio 35 μm Pitch Through-Wafer Copper Interconnects by Electroplating for 3-D Wafer Stacking

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We report the fabrication of high aspect ratio (~15) ultradense (~80000/cm^2) through-wafer copper interconnects by a special aspect ratio dependent electroplating technique. In this approach, electroplating process parameters were continuously varied along with varying unfilled via depth, to maintain the uniform current distribution and thus uniform metal deposition. Copper interconnects, with diameters as small as 12 μm and a pitch of 35 μm, were electroplated without any voids. Due to ultrafine pitch and extremely high number of I/Os per cm^2, these interconnects were found to have significant potential in three-dimensional (3-D) wafer stacking and other high-density electronic packaging applications.
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The demands of fabricating cheaper, smaller, and lighter electronic products offering better performance and increased functionalities are continuously growing. The number of electronic devices on a single chip is rapidly increasing, and thus initiating the need of multilevel interconnections. According to International Technology Roadmap for Semiconductors (ITRS) 2005, integrated circuit (IC) chip size will be in the order of 30 nm by 2010. Such a nanosized IC will carry more than 100 million transistors, which will further require more than 100,000 I/Os for next level packaging. To accommodate such a huge number of I/Os in constantly reducing package size, novel approaches, such as wafer stacking, are needed to fabricate interconnects having a pitch size as low as 20 μm.

Three-dimensional (3-D) wafer stacking represents a wafer level packaging technique wherein specific components, such as logic, memory, sensors, A/D converters, etc., are fabricated on separate wafer platforms and then integrated onto a single wafer-scaled package using through-wafer interconnect (TWI).[2-5] Because these devices are interconnected in the vertical axis, the electrical signal path becomes shorter, which results in lower parasitic losses, lower power consumption, and better system performance. Fabrication of these TWIs by electrodeposition and other techniques has been reported in the literature.[2-8] Although several conductive materials such as gold,[3] polysilicon,[4,5] and Sn-Pb solder[8] have been used as interconnect material, copper is the best choice due to its higher electrical conductivity and electromigration resistance.[6,7] For the purpose of depositing metal in deep through-holes, electroplating is the most widely used process.[6-8]

Although the earlier reported interconnects have shown satisfactory performance, fabrication of very high aspect ratio (>10) interconnects having ultrafine pitch (~20 μm) still remains a challenge.[6] Two main hurdles in the way of fabricating high aspect ratio interconnects are the uneven local current density distribution inside the through-holes and insufficient wetting of via surface with copper electrolyte. In high aspect ratio through-hole plating, current distribution does not remain uniform along its depth; current is higher at the inlet and outlet of through-hole. As a result, metal deposition is greater at the corners than in the center, which results in void formation in the center and bottom of through-vias.[9]

Inadequate interaction between via surface and copper electrolyte is the other critical reason behind the void formation problem in high aspect ratio electroplating. When via sizes are a few micrometers and several hundred micrometers deep, via surface characteristics play a critical role in deciding the metal distribution phenomenon. In very deep and narrow through-holes, electrolyte does not wet via surface completely and in some cases even does not reach at some local via points. At present, deep reactive ion etching (DRIE) is the most common technique to make high aspect ratio through-vias. During the passivation step of DRIE process, a thin layer of polymer poly(tetrafluoroethylene) (PTFE) is deposited on the sidewalls, which protect the sidewalls from lateral etching and produces vertical profile. However, PTFE is a hydrophobic material and thus it reduces the wetting of via surface with copper electrolyte. Due to insufficient wetting of copper electrolyte and local via surface points, current density distribution varies which results in nonuniform copper deposition along the through-via surface. To fill copper without any voids, the hydrophilic characteristic of the via surface must be enhanced, so that via surface can be properly wetted by copper electrolyte.[10]

In addition to these issues, wafers often need to be thinned down, as present electroplating techniques are able to fill through-holes having a limited aspect ratio. This thinning down requires additional polishing and expenses, hence efforts are ongoing to develop electroplating processes that can fabricate very high aspect ratio, fine pitch through-wafer interconnects in normal thick wafers and thus avoid the wafer thinning process.

In this paper, we report the fabrication of high aspect ratio (>15) through-wafer copper interconnects, having pitch sizes as small as 35 μm, by a special aspect ratio dependent electroplating technique.[11] The diameter of the fabricated copper interconnects is in the range of 12–30 μm, while their height is from 200–400 μm. These electroplated copper interconnects will be used in the fabrication of 3-D MEMS/IC device.

A schematic diagram showing the concept of such a 3-D wafer stacked device using through-wafer electroplated copper interconnect is shown in Fig. 1. As depicted, several electronic devices will be stacked vertically using solder bumps and through-wafer copper electroplated interconnects. Because these devices are vertically stacked, the cross-sectional war page area of the device will be extremely compact and a larger number of devices can be placed in the same chip area.

Experimental

Making vertical through-holes with smooth sidewalls in silicon is one of the most important fabrication steps. In the past, several methods, such as wet etching, electrochemical etching, and laser drilling have been used to create through-holes DRIE, however, is found to be the most suitable process. DRIE creates almost vertical through-holes with relatively smooth surfaces at high etch rate.[6,7,12] Similarly, complete filling of conductive material in the through-holes is a very crucial step for fabricating through-wafer interconnects. Incomplete metal filling and void formation inside the vias will lead to short-circuiting and will affect the electrical perfor-

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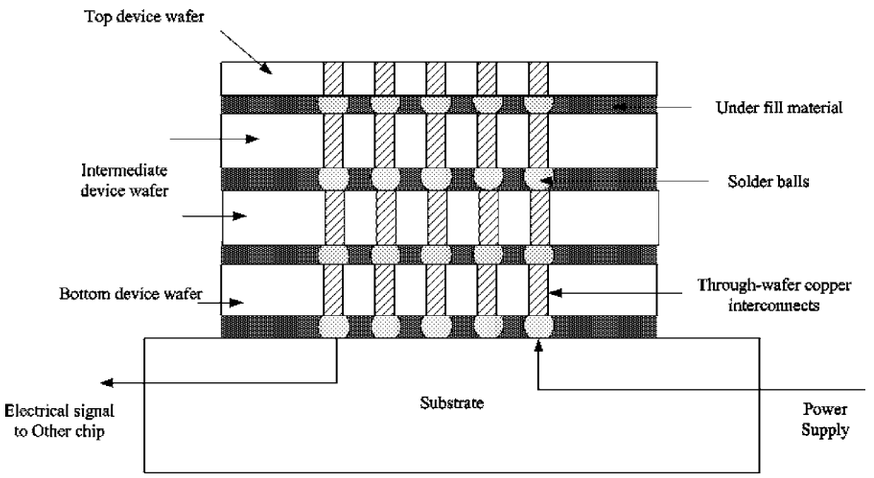

Figure 1. Schematic representation of 3-D wafer stacked device.

mance of the overall device. Grain size of deposited metal is also very critical as grain roughness directly affects the electrical properties such as electrical resistivity, electromigration resistance, etc. Rough grains may also lead to mechanical failure as stress concentration is high at those local points. Thus, smooth, void free, fine grain metal deposition in high aspect ratio through-vias is essential.

In the present experiments, we used bottom-up electroplating technique to electroplate through-wafer interconnect. At first, through-holes of varying diameters ranging from 10 to 30 μm were etched through in 200–400 μm thick silicon wafer in STS DRIE etching tool. AZ9260 photoresist (10 μm thick) was used as an etching mask. Flow rates of etching gas (SF_6) and passivation gas (C_4F_8) were 120 and 85 sccm, respectively, while the coil and platen power were 600 and 160 W, respectively. Average silicon etching rate was found to be varying from 1.5 to 2.5 μm/min, for different via openings. After the etching process, a 200 nm insulation layer of silicon nitride was deposited in through-vias to prevent the diffusion of copper in silicon. A 300 nm gold seed layer was deposited by sputtering process along with 20 nm Cr adhesion layer.

Bottom-up electroplating technique was used in a home—designed electroplating setup to deposit copper in DRIE etched through-vias. Copper electrolyte was provided by Atotech (Germany). This electrolyte has three main components: a base solution containing copper sulfate, sulfuric and hydrochloric acids, and organic additives, i.e., brightener and leveller. The following is the optimum concentration of these ingredients: copper 40 g/L, sulfuric acid 150 g/L, chloride 50 mg/L, leveller 15 mL/L, and brightener 10 mL/L. Total electroplating time in filling the through-vias was ~30 h. After electroplating, cross sections of the through-wafer electroplated vias were characterized by scanning electron microscope (SEM).

Results and Discussion

From the experiments it was found that complete wetting of via surface with electrolyte is very critical for uniform metal deposition.[11] To improve the interaction of via surface with electrolyte, we have investigated the wetting characteristics of commonly used insulation materials with copper electrolyte, and the effect of various surface treatments in improving their wetting behavior. The surface treatment method includes cleaning in SC1 solution (30% H_2O_2, 25% NH_4OH, and deionized (DI) water in 1:1:5 ratio) at 75°C for 30 min, followed by DI water rinsing and nitrogen drying. Contact angles of these samples with copper electrolyte were measured, both prior and after the surface treatment.

Figure 2 gives the summary of contact angle of common insulating materials with copper electrolyte. It is evident from this figure that most of the sample surfaces are of hydrophilic in nature (contact angle less than 70°). The contact angle of the thermally grown SiO_2 sample was found to be 69°, which shows the hydrophobic nature of SiO_2. The contact angle of DRIE etched silicon sample with copper electrolyte is also higher (47°), which is due to polymer deposition in passivation cycle. It was found that the contact angle of the samples reduced significantly after SC1 surface treatment. SC1 surface treatment increases the surface area, which absorbs more of the functional group. Common functional groups absorbed on the surface are hydroxyl (-OH group) and amino ($-NH_2$) group, which comes from SC1 solution (30% H_2O_2, 25% NH_4OH). After SC1 treatment, the contact angle of DRIE etched silicon with SiO_2 and Si_3N_4 was found to be only 3°, thus making it the most suitable insulating material for electroplating, compared to conventional SiO_2 insulation layer.

In these experiments we have used aspect ratio dependent electroplating technique to fill copper in through-holes. This technique is based on the continual changing unfilled depth of through-vias. Due to continuous metal deposition in the electroplating process, the interelectrode gap gradually reduces. This continual reduction in interelectrode gap affects the electrolyte kinetics and cupric ion mass transfer. Primary and secondary current distributions, which are the result of ohmic potential drop through the electrolyte and various polarization effects, respectively, depend upon the interelectrode gap. Current distribution increases when the interelectrode gap reduces. As a result of continual reduction in effective unfilled depth or interelectrode distance from anode, the current distributions inside the deep through-hole become nonuniform. This nonuniformity in current distribution and mass transfer of cupric ion affects the copper deposition and results in void formation, incomplete filling, rough grain formations, and other undesired results.

In aspect ratio dependent electroplating technique, the electro-

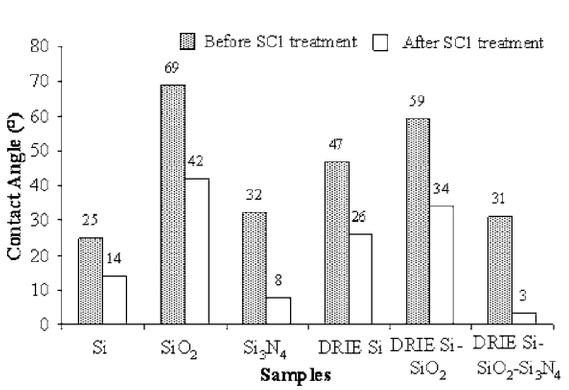

Figure 2. Contact angles of samples prior to and after the surface treatment.

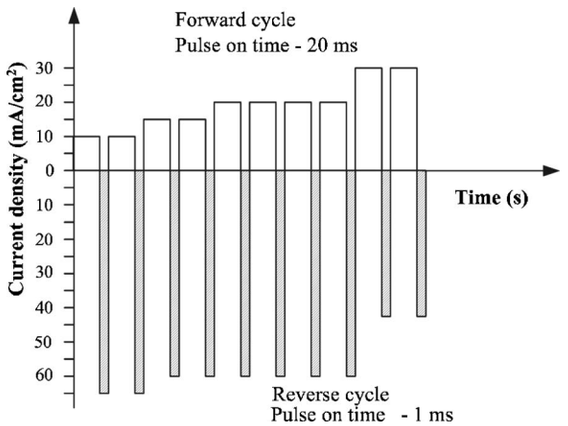

Figure 3. Variation in forward and reverse current density with electroplating time.

plating parameters were varied along with the continually changing unfilled depth, thus maintaining the uniform current distribution.[11] In the beginning of the electroplating process, relatively low forward current density (10 mA/cm^2) with high reverse current density (60 mA/cm^2) were used so that copper grains can be deposited without any voids (Fig. 3). In reverse pulse on period, reverse current removes copper from predeposited locations, thus making the metal distribution more uniform. As the electroplating process continues, forward current density was gradually increased in steps (12, 15, 20, 30, and 60 mA/cm^2) while reverse current density was reduced (60, 50, 45, and 30 mA/cm^2). Pulse on time in forward cycle was reduced from 40 to 20 ms, while pulse on time in reverse cycle was kept constant, i.e., 1 ms (Fig. 3).

The combined effect of enhanced wetting characteristics and improved current distribution resulted in uniform plating and fabrication of smooth copper pillars. Figure 4 shows a 20 $\times$ 20 array of freestanding copper interconnects having a pitch size of 35 μm. The diameter of each copper pillar is $\sim$15 μm, while its height is 225 μm. Silicon between the copper pillars was dissolved by KOH solution to show the outer surface and electroplated grains. Pitch size between the copper interconnects is 35 μm, which means that more than 81,600 I/Os per cm^2 can be incorporated. The aspect ratio of the fabricated through-wafer copper interconnects by electroplating is more than other reported results in similar area.

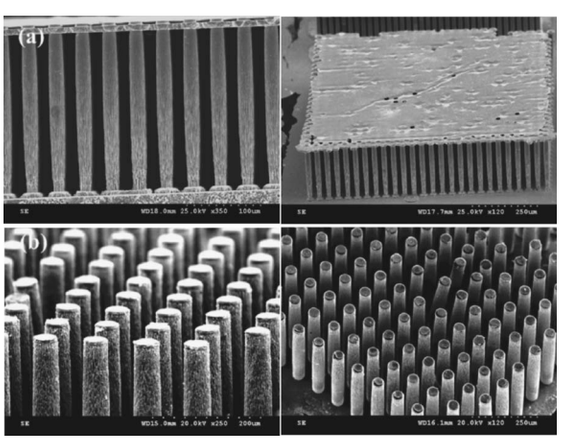

Figure 4. High aspect ratio through-wafer copper interconnects after the dissolution of silicon. (a) Diameter 15 μm, pitch size 35 μm, aspect ratio 15. (b) Diameter 30 μm, pitch size 80 μm, aspect ratio-12.

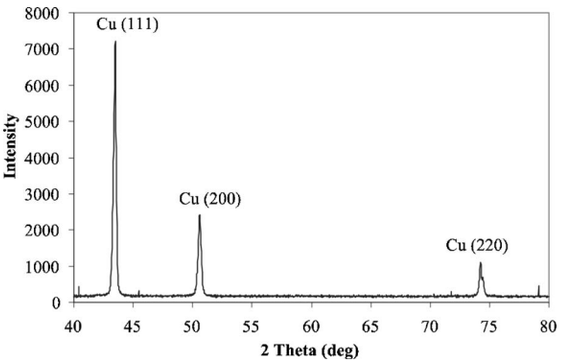

Figure 5. XRD analysis showing ⟨100⟩ crystal orientation of copper electroplated interconnects.

As illustrated, the copper interconnects are vertical and smooth. Interconnect diameter is more at the center and the surface is rougher at the bottom, which is caused by various DRIE effects termed as bowing and RIE-lag, respectively. Copper interconnects having diameters of 30 μm and pitch of 80 μm, are shown in Fig. 4b. One of the important features of this special electroplating technique is its ability to produce identical copper interconnects in large number. As demonstrated in the SEM images, copper grains are elongated in vertical direction, which is the prime characteristics of bottom-up electroplating approach.

The electroplated copper interconnects in our experiments are polycrystalline in nature. X-ray diffraction (XRD) analysis of the electroplated copper grain revealed that the crystal orientation of most of the electroplated copper grains is ⟨111⟩ plane (Fig. 5). As electromigration and stress migration resistance of ⟨111⟩ texture are the maximum,[13,14] these electroplated copper interconnects can be used in high current density applications. The electrical conductivity of the electroplated copper interconnects was measured by a two-point resistance measurement. The average electrical resistivity was found to be 8.26 $\times$ 10^{-7} Ω-cm. The measured electrical conductivity of electroplated copper is less than the bulk value of copper (1.67 $\times$ 10^{-7} Ω-cm), which is due to the recrystallization of copper grains at room temperature.[15,16] Oxide formation on the surface of copper interconnects is another possible reason for the increased electrical resistivity. Although the measured electrical conductivity is less than the bulk value, it is still satisfactory for 3-D IC/MEMS packaging applications.

While conventional pulse reverse electroplating technique is able to fill copper in through-holes having aspect ratio only on the order of 10, this new approach is able to fabricate interconnects having aspect ratios as high as 15 with ultrasmall pitch, thus shows potential to achieve the goal set by ITRS roadmap. Experiments are ongoing to fabricate ultracompact 3-D IC/MEMS devices using through-wafer copper interconnects having an aspect ratio greater than 30 with a pitch less than 10 μm.

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