

# Electroless and electrolytic copper plating of glass interposer combined with metal oxide adhesion layer for manufacturing 3D RF devices

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**Abstract**—High performance radio frequency (RF) front end filters were fabricated using glass interposer and 3D packaging technologies, especially through glass vias (TGV) and direct Cu metallization on the glass.

Major challenges for the use of TGV in RF and electronics applications are the cost competitiveness, high throughput and reliable metallization of both TGV and flat glass surface with an excellent adhesion.

In this study, a thin metal oxide adhesion promotion layer (about 8-9 nm) called VitroCoat layer is dip-coated by a modified sol-gel process followed by sintering which creates chemical bonds to the glass. Sol-gel dip coating process has good coating uniformity on both TGV and top surface under optimized coating conditions. Uniform coating can be achieved on minimum 30  $\mu\text{m}$  diameter TGVs on a 300  $\mu\text{m}$  thick and 200 mm diameter glass wafers. The thin adhesive layer enables electroless and electrolytic copper plating directly onto glass substrates without impacting high frequency performance. Excellent adhesion of electroless plated copper seed layer on glass can be achieved by using the adhesive layer and annealing technology. The thin adhesive layer is non-conductive and can be easily removed from the area between circuit traces during electroless copper seed layer etching.

We have successfully integrated the adhesion layer and electroless and electrolytic copper plating technologies into semi-additive process (SAP) and built up a 3D RF front end filter devices on 400  $\mu\text{m}$  thick 200mm diameter glass wafers as well as 300mm x 300mm glass panels with 80  $\mu\text{m}$  diameter holes.

*Keywords*- Glass interposer; metal oxide adhesion layer; 3D RF passives; wet Cu metallization

## I. INTRODUCTION

With the recent commercialization of carrier aggregation, RF far front end filters require reduced size of inductors and capacitors while keeping high quality factors. High performance RF multiplexers have low insertion loss and rejection at certain frequencies which can be achieved by reducing the electromagnetic coupling between components. To meet this stringent filter requirement three-dimensional (3D) RF inductor-capacitor (LC) filters have been fabricated on through-glass-via (TGV) and on a glass substrate surface [1]. The inductors were formed by metalizing TGV. On top of high-Q TGV inductors traces as a capacitor bottom plate, high-Q copper MIM (metal-insulator-metal) capacitors were integrated by depositing a silicon nitride dielectric layer followed by another thick Cu plating as a capacitor top plate.

The attraction of glass as interposer substrate is from a list of important advantages including superior dimensional stability and CTE matching to silicon chip that lower the risk of warpage [2], smoothness of glass surface which enable fine line patterning. Glass has inherently superior electrical properties to silicon such as low dielectric constant and loss tangent which is beneficial to high frequency application. Electrical characterization and electrical models has demonstrated the advantages of the insulating properties of glass, and its positive impact on functional performance [3]. In addition, through holes have been fully patterned on glass substrates in the form of wafer and PCB panel which enables high throughput and large volume production.

Unlike organic substrate it is challengeable to metalize glass surface because smoothness of glass has low chance to form mechanical anchoring between metal and glass like organic substrate to provide good adhesion [4]. Therefore it

is desirable to have an effective adhesion promoter between metal and glass to provide good adhesion while not changing the mechanical and electrical properties of glass. Physical metal deposition technique such as physical vapor deposition and sputtering deposition has been widely used for metalizing silicon wafers in semiconductor industry. This technique has also been applied on glass surface metallization by depositing tens of nanometer titanium or chromium as an adhesion layer prior to bulk metal deposition [5].

For metalizing glass surface, TGVs and blind glass vias with copper we have developed a metal oxide adhesion promotion layer which can be dip coated conformally on the inside wall of TGVs and glass top surface by a modified sol-gel coating technique. The adhesion layer allows electroless copper plated directly on glass as a seed layer and then electrolytically plating thicker copper [6], [7]. This wet metallization combined with annealing procedures can give excellent adhesion between electroless copper and glass. Adhesion layer coating, electroless copper plating, photolithographic patterning and electrolytic plating to form conducting circuits (so called semi-additive process, SAP) have been integrated seamlessly to the process of fabricating 3D RF devices in wafer and panel scales.

The advantages of the panel scale metallization on glass are ease of realizing high throughput mass production using current PCB, LCD, flexible display and solar panel infrastructures and low equipment investment and cost of ownership which can significantly reduce the cost of the final product. In addition, this wet chemical metallization is a double side process resulting in cost reduction and simplifying the procedures.

This paper will focus on the process technology challenges on wafer and panel scales in terms of coating uniformity, TGV blockage, electroless adhesion evaluation and the copper thickness uniformity and throwing power of the electrolytically pattern plating. The electrical performance and the reliability of chip level conditioning have been evaluated as well.

## II. METHOD AND PROCESS

### A. Materials

Glass substrates in slide, wafer and panel shapes with or without TGVs were manufactured by Corning Incorporated. The glass substrates before adhesion promoter application were precleaned by EXPT Vitrocoat GI PreClean-1 (Atotech).

### B. Adhesion promoter coating and SAP process flow

The critical process of fabricating a 3D RF device is the copper metallization of TGVs and the smooth glass surface. The core process steps are applying the adhesion promoter followed by the SAP metallization process. Figure 1 shows the process flow chart.

1) *Adhesion promotion layer formation:* Glass substrates with or without TGVs were precleaned with

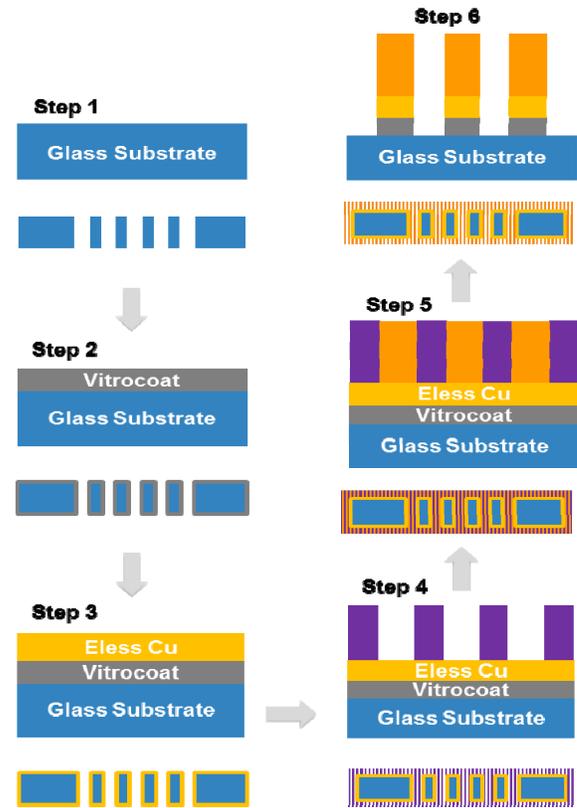


Figure 1. Cu metallization on glass surface and TGVs by adhesion layer application and SAP

EXPT VitroCoat GI PreClean-1, as shown in step 1 (Figure 1). This is done to remove any organic and inorganic residue on the glass surface and prepare a clean surface for the following coating step. The precleaned substrates were dipped in a Vitrocoat GI (Atotech) solution containing the adhesion promoter precursor. By pulling out the sample at a specific speed a uniform layer was formed on the glass surface after the solvent evaporated. A prebaking step was applied on the coated layer to remove the solvent furtherly. To form the final adhesion layer a high temperature sintering step is necessary. The thickness of the adhesion layer is adjustable by changing precursor concentration, pulling out speed and number of repeating dipcoating/prebaking step.

2) *Electroless copper seed layer plating:* This process formed a thin copper seed layer on the adhesion layer as shown in step 3 (Figure 1). The adhesion promoter coated glass substrates were activated by a palladium catalyst and finally plated in an electroless copper bath (Atotech CupraTech GI). The thickness of the electroless copper is controlled usually in the range of 400–450nm. An annealing of the electroless copper deposit was done to improve further the adhesion.

3) *Photolithographic patterning:* Dry film photoresist patterns were formed on the electroless copper seed layer as

shown in step 4 (Figure 1) by dry film lamination, light exposure, development and dry film residue cleaning.

4) *Electrolytic copper pattern plating*: Copper was plated electrolytically to a thickness of 13  $\mu\text{m}$  on the electroless copper seed layer. This is a double sided conformal plating process and requires a plating bath setup having good coating uniformity in thickness and strong throwing power inside of TGVs.

5) *Circuit formation*: Step 6 in Figure 1 is the last step of SAP process consisting of stripping off dry film photoresist, electrolytic copper annealing and differential etching of the electroless copper seed layer and adhesion layer. Noted that here the adhesion layer can be removed with the same etching solution as electroless copper seed layer in one step.

### C. Measurement tools and methods

The thickness uniformity of the adhesion layer on flat substrate was investigated by X-ray fluorescence (XRF) mapping. The TGV blockage was evaluated under backlight optical microscope and defined by the percentage of blocked vias out of the total vias investigated. The interface of ultrathin layer was observed with energy filtering transmission electron microscope (EF-TEM).

The cross sectional samples were prepared by epoxy casting, grinding and polishing. The samples were investigated by optical microscope.

## III. RESULTS AND DISCUSSION

### A. Coating quality of the adhesion layer on a flat glass surface and within TGVs

#### 1) Dip coating uniformity

Among of many approaches for the thin metal oxide layer deposition like spray pyrolysis, spin-coating or chemical vapor deposition, the dip-coating approach is an easily

controllable and cost-effective method for glass substrates with TGV structures in high throughput and large panel scale.

Ultra-thin layers of less than 10 nm can be achieved at specific pulling-out speed at reduced material consumption. The size of the samples which can be dip coated varies from small glass slides, 200 mm diameter glass wafers and the full panels with the sizes up to 508mm x 508mm. Glass slides coated with the adhesion layer has been mapped with XRF at 3.0mm slit/15sec. The measured thickness value is  $9.0 \pm 1.0 \text{ nm}$ . The x-section of the adhesion layer was characterized by EF-TEM and as can be seen in Figure 2. It was shown that the adhesion layer is about 8-9 nm thick and uniform.

#### 2) Coating capability on TGVs

If the dip coating technique is used for large areas of flat substrates without any structure, there is usually no problem in terms of the coating uniformity and the film quality. But it is quite challenging to get a uniform conformal coating inside of TGVs and on top of the surface, especially for high aspect ratio vias and small via diameter. This is partially due to surface tension difference between the top flat surface and the inside of TGVs. Additionally, TGV blockage could occur if the cleanliness of the glass surface, concentration of precursor and physical properties of coating solution, pulling out speed and coating environment such as temperature or relative humidity are not at optimized conditions. The mechanism of TGV blockage is being investigated. A possible explanation is the coating will be thinner at the outside corner and thicker at the inside corner due to the free surface contacts to minimize the surface energy when a liquid coating is applied on a curved surface [7], [8]. A multiple component containing coating solution makes the dynamics of the thinning process even more complicated. Compositional changes in the bulk liquid during drying and convection of other additives will cause surface tension gradient effects. Due to solvent evaporation the viscosity varies which makes the liquid exhibit shear-thinning rheology. Moreover, capillary force tends to draw more solution into TGVs and the adhesion promoter precursor can recrystallize during solvent evaporation and thus lead to blockage in TGVs. It was found that this effect depends on the aspect ratio, via diameter and density of TGVs.

A series of TGVs with different diameter, aspect ratio, via shape and via pitch have been dip coated with Vitrocoat GI S-1 and evaluated under backlight optical microscope. For blockage investigation the adhesion layer was covered by conformally plated electroless copper. The copper blocks the light and thus helping to determine the blockage of TGVs under backlight microscope.

Under optimized coating conditions no blocked TGV was observed with aspect ratio up to 30:1 and via pitches

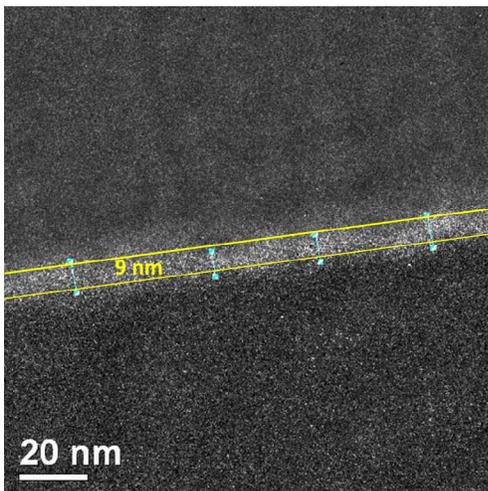


Figure 2. EF-TEM image of adhesion layer

from 40 to 200  $\mu\text{m}$ . The thickness of TGV substrates being evaluated is from 200-400  $\mu\text{m}$ .

Figure 3 shows some representative backlight optical microscope images on the TGV after coated with adhesion layer and electroless seed layer. Regardless of via size, aspect ratio, via pitch, all of TGVs listed are free of blockage.

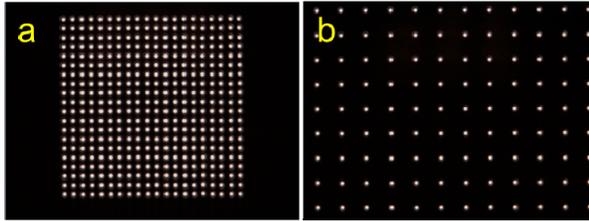


Figure 3. Backlight optical microscope images on TGVs coated with adhesion layer and electroless copper plating. a) Aspect ratio=11:1 and pitch=50  $\mu\text{m}$  and b) Aspect ratio=4.5:1 and pitch=101  $\mu\text{m}$ .

### B. Electroless copper seed layer plating

It is important to have a uniform copper seed layer on the surface and inside of TGVs to get a high quality of conformally plated electrolytic copper in the SAP process. If the copper seed layer is too thin at the center of the inside of TGVs plating defects might occur. Figure 4 displayed the pictures of glass wafers and panel with TGVs after deposited with electroless copper seed layer. There is no delamination or blistering on electroless



Figure 4. Pictures of wafer and panel glass substrates after electroless copper plating

copper seed layer before and after annealing. The seed layer passes the hatched tape test.

### C. Electrolytic copper pattern plating

After depositing the electroless copper seed layer and photolithography a double sided electrolytic copper pattern plating step was conducted to deposit the thick copper layer for circuitry. The requirement for this step includes high throwing plating power in TGVs, low surface overburden, high thickness uniformity across wafer or panel and good adhesion of copper to glass substrate.

### 1) Process compatibility

Figure 5 shows the images of a whole wafer and patterns after photolithographic patterning, electrolytic copper plating and dry film resist removal. Comparing the image a) to b) before and after pattern plating no process issue such as blister, resist pattern lifting off, skip plating or other defects was observed. This demonstrates the compatibility of plating bath chemicals and processes to the dry film resist patterns. Figure 5c shows the electrolytic copper patterns with electroless copper seed layer after dry film resist removal. No lifting off of copper trace and seed layer occurs.

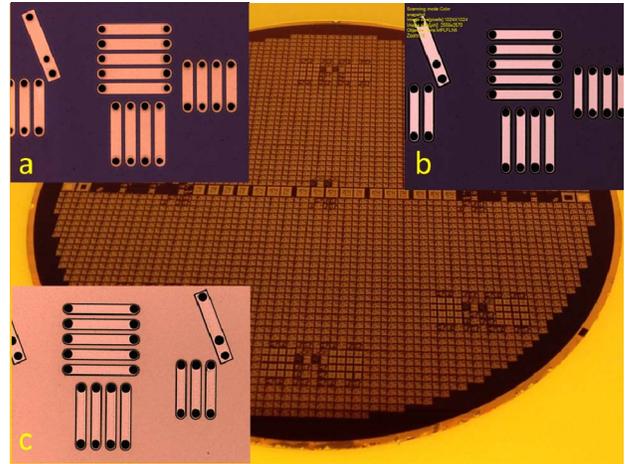


Figure 5. Images of electrolytic copper pattern plating a) post photolithographic patterning; b) post electrolytic copper plating; c) post dry film resist removal and the whole 200mm wafer.

### 2) Throwing power

The throwing power for through hole or blind micro via filling and conformal plating is a key criterion for evaluating the plating bath and optimizing the plating parameters.

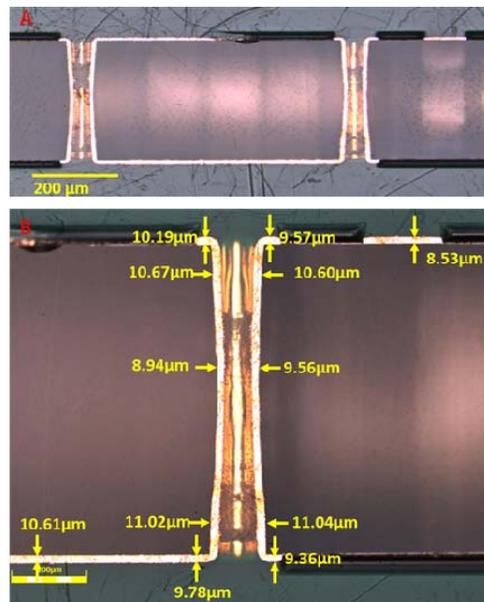


Figure 6. Cross sectional images of metallized TGVs

The throwing power depends on the composition of brightener and leveler and other additives in the plating bath. The applied voltage, current density and the configuration parameters of anodes and cathodes in plating bath are also important for a good quality deposit. To evaluate the conformal plating quality of TGVs, the cross sectional analysis of TGVs has been done with laser confocal microscope. Figure 6a showed the cross sectional images of two adjacent TGVs after pattern plating before dry film resist removal. No void or blister was observed inside of TGVs. For throwing power calculation the copper thickness of more than ten spots was measured as shown in Figure 6b. The throwing power on the TGV is 103%. The throwing power varies on the location of TGVs within one wafer and wafer to wafer. To reduce the variation of throwing power the plating bath design needs to be improved.

### 3) Copper thickness distribution on wafer for pattern plating

Two methods have been used for copper thickness measurement. One is using laser confocal microscope to acquire the image on the dry film resist patterns before and after pattern plating and then measure the heights of the patterns with depth profile measurement software. The difference of the pattern height before and after plating is the thickness of electrolytic copper. This method is simple and fast and nondestructive to samples. The other method is measuring copper thickness on cross sectional images acquired by confocal microscope on every spot. This method is more accurate but time and labor consuming and not suitable for samples in the downstream process. Two methods have been compared by measuring both sides of one wafer and 12 spots evenly distributed on each side. The off-set of the average copper thickness between two methods is less than 10%. Therefore, the depth profile measurement on dry film resist pattern was chosen to evaluate the copper thickness distribution on the wafer.

Table I lists copper thickness data on both sides of four 200mm diameter wafers after pattern plating with the target thickness of 13  $\mu\text{m}$ . The standard deviation varies from 0.7 to 2.16  $\mu\text{m}$  which is acceptable for laboratory scale plating bath. A 300 mm x 300 mm glass panel with 400  $\mu\text{m}$  thick has been pattern plated with panel scale plating bath.

TABLE I. COPPER THICKNESS ON BOTH SIDE OF WAFERS

Wafer No.	Side A		Side B	
	Average	STDEV	Average	STDEV
1	12.86	2.16	14.20	1.70
2	11.75	1.33	14.15	2.02
3	12.17	0.71	13.99	1.30
4	10.78	1.00	12.51	1.22

Note: 6 spots were measured on each side of wafer, the unit is  $\mu\text{m}$

Table II lists the copper thicknesses measured on 9 spots evenly distributed on the 300 mm x 300 mm area. The copper thickness is  $12.1 \pm 0.6 \mu\text{m}$  on the top and  $12.1 \pm 0.7 \mu\text{m}$

at the bottom. The uniformity of the pattern plated copper thickness on the glass panel is satisfying.

TABLE II. COPPER THICKNESS ON BOTH SIDE OF PANEL

Spot	1	2	3	4	5	6	7	8	9
Top	11.6	12.9	11.1	11.9	12.3	12.7	12.6	11.4	12.0
Bottom	11.4	12.2	11.9	11.8	12.4	13.1	13.0	12.0	11.2
Average	Top = 12.1		Bottom = 12.1						
STDEV	Top = 0.6		Bottom = 0.7						

Note: the unit is  $\mu\text{m}$

### D. Dry film resist removal and differential etching of electroless seed layer

After pattern plating dry film resist patterns were removed by resist stripper and followed by an annealing step to release the internal stress of electrolytic copper. A proper copper etchant has been used to remove electroless copper seed layer and adhesion layer.

### E. Reliability and electronic performance of 3D RF devices fabricated by SAP process

During the glass double-side and TGV sidewall simultaneous plating for the high-Q 3D inductor formation, capacitor bottom plates were also formed on one side of the glass substrates. On top of the thick Cu traces, the capacitor dielectric material such as Silicon Nitride were deposited and patterned on the capacitor area. After that, capacitor top electrodes were formed by another Cu-plating using the SAP process. Both inductors and capacitors were then connected to form a desired LC network, by putting passivation, contact via opening, and final interconnect metallization. Figure 8a and 8b are the photos of a 200 mm diameter wafer and a 300 mm x 300 mm panel with devices fabricated by SAP process. After final passivation, the wafers were ball attached and singulated as a stand-alone RF front end filter as shown in Figure 8c and 8d.

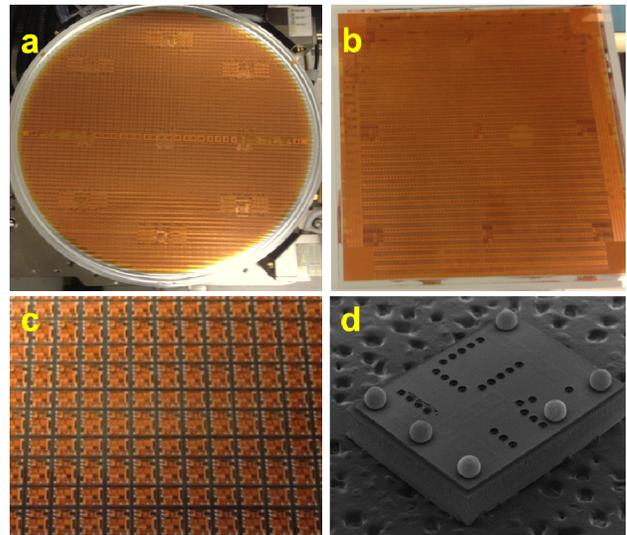


Figure 8. Images of wafer and panel samples after fabrication of 3D RF filters including inductors and capacitors. a) 200mm diameter wafer; b) 300 mm x 300 mm panel; c) 3D RF device after ball attachment and d) the device after singulation

The diced filter devices went through chip-level reliability conditioning, including thermal cycles, high-temperature storage (HTS), and highly accelerated stress test (HAST). The devices were electrically and mechanically characterized before and after the reliability preconditions, showing robust process and device integrity of the batch processed new adhesion layer and Cu plating with the remaining integrated passive device (IPD) fabrication and wafer-level packaging (WLP) processes.

#### IV. CONCLUSION

The adhesion layer coated on glass allows electroless copper seed layer plating on glass with good adhesion to fulfill the whole SAP process for 3D RF device fabrication. The adhesion promotion process is a robust, high throughput and cost effective method of electroless plating of copper on flat glass surface and TGVs. Robust throwing power allows the uniform conformal coating of TGV aspect ratios up to 30:1 in a reliable manner. The process has been successfully applied on copper metallization on TGVs in both wafer and panel scales. The 3D RF devices made with this process have good electronic performance and reliability.

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