

Fan-out packaging: a key enabler for optimal performance in mobile devices

By Cassandra Melvin, Roger Massey [Atotech Deutschland GmbH]

As technology becomes more advanced and innovative, smartphones are increasingly thinner and are adopting larger, higher definition displays, while providing higher speed connections with better overall power efficiency. All just to satisfy our never ending demand for faster, higher tech devices, with maximum battery life [1]. Advanced packaging technologies, and in particular fan-out wafer-level packaging (FOWLP), enable manufacturers to deliver these features by overcoming key processing challenges using packaging innovation.

The emergence of FOWLP has been directly linked to satisfying the changing requirements for consumer electronics, and particularly those of mobile devices. This article will explore the drivers behind fan-out packaging, the key processing challenges, and the requirements at the application level. It will also discuss why fan-out is the ideal packaging technology for future generation mobile devices, and will present a turnkey electroplating solution for manufacture within both the current wafer, and the much anticipated larger panel format.

Smarter mobile phones require innovative approaches to both IC manufacturing and packaging. Moore's law has been pushed to its limit and is being surpassed by a new momentum for "More than Moore." This new approach to advancing technology requires packaging solutions to push technical boundaries and enable increased integration and performance, with fan-out packaging being considered as an ideal technology to achieve this.

What is fan-out packaging?

A fan-out package can be defined as IC packaging wherein the interconnections are fanned out of the chip area and therefore bumping is not dependent on the die surface [2]. Another distinguishable feature is that fan-out packages use an epoxy mold compound to fully embed the dies, rather than placing them upon a substrate or interposer as in other packaging types.

There are a variety of fan-out packaging types, with varying levels of integration and architecture complexity.

While the FOWLP process sequence varies from one manufacturer and packaging variant to the next, the baseline processes are generally comparable. An adhesive material is applied to a carrier wafer and one or multiple die are then placed face down onto the adhesive layer. This is followed by a wafer-level over-molding, which essentially embeds the die(s) into the molding layer. Debonding is next in the process, during which the carrier wafer is removed from the newly reconstituted over-molded wafer, thus exposing the active area of the die. Redistribution layer (RDL) formation is next, which occurs across the increased area of the over-mold, followed by soldering, and finally die singulation [2].

For current and next-generation mobile devices, ultra-thin and high-density packages are needed. Fan-in package types known as wafer-level chip-scale packages (WLCSP) had previously been the preferred technology for smartphones (Figure 1), as the package offers a relatively small

form factor and footprint. The downside, however, is that WLCSP tends to have limited I/O count (approximately 200) and a minimum package profile of 0.6mm [3]. When dealing with a pitch shrink, CSP suffers processing challenges as the area available for I/O layout is limited to the die surface. Fan-out packaging, however, does not have this limitation as the technique allows for the redistribution of I/Os beyond the die surface and onto the over-mold which, in turn supports a thinner package which, in turn supports a thinner package down to 0.4mm [3]. The benefits of a higher I/O density and thinner package will be discussed in the next section.

Fan-out: key drivers

Key drivers for the industry to pursue fan-out packaging technologies are discussed in the following sections.

Better performance. Mobile devices, and particularly smartphones, have become ubiquitous in our daily lives. Smartphones are no longer considered to be phones, but rather pocketable, personal computers; it's been reported that nearly 80% of smartphone owners reach for their phone within the first

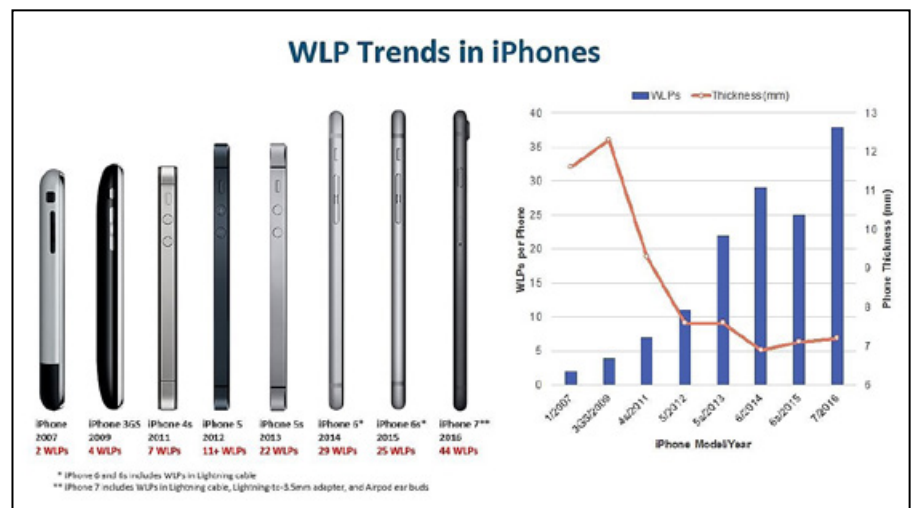


Figure 1: The image shows the decreasing thickness of handsets and the increasing number of wafer-level chip-scale packages (WLCSP), a fan-in technology. Some of these CSPs may be replaced or integrated into FOWLP for future generations of mobile devices. SOURCE: TechSearch International

fifteen minutes of being awake, and spend an average of 132 minutes communicating on their smartphone throughout the day (Figure 2) [4]. To support such a high level of activity, a smartphone must be robust and offer best in class performance.

For microprocessors, best in class performance refers to optimized reliability, including both thermal and electrical performance. Product or component

Additionally, more physical connections to the printed circuit board (PCB) enable better heat flow, which is critical for thermal performance. Power dissipation is necessary to effectively remove the heat generated by the IC when in use, as overheating due to poor power dissipation leads to IC malfunction and/or destruction. This is particularly critical in mobile devices where heat management is an issue.

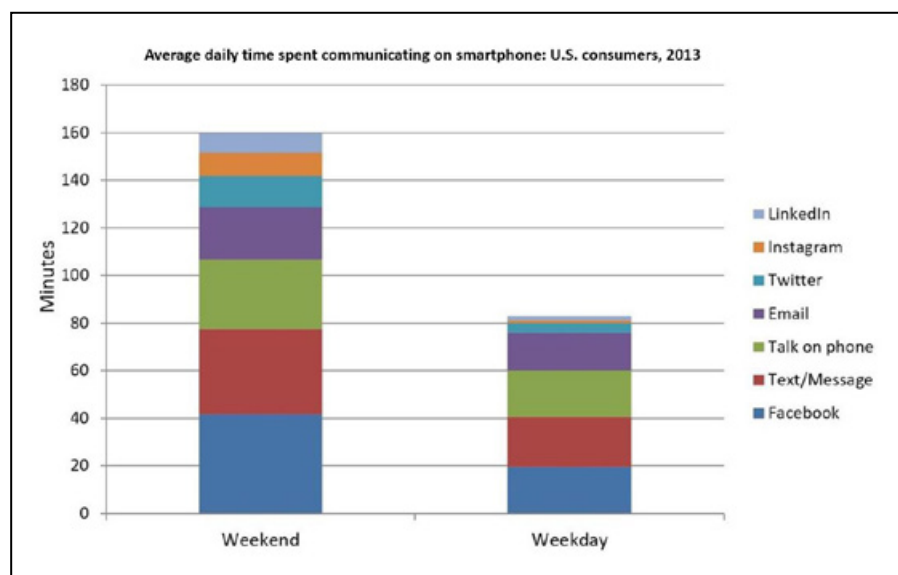


Figure 2: The diagram shows the average daily time spent communicating on smartphones according to [4].

reliability performance ultimately determines the lifetime of the device, as well as its ability to perform multiple tasks quickly, concurrently, and consistently over an extended period of time. As such, one key measure of any package is electrical performance. Where multiple die are embedded in a single FOWLP, when compared to other packaging techniques, the overall electrical path is shorter, resulting in faster signal transmission and improved electrical performance. This provides a considerable technical advantage and positions FOWLP as an ideal technology for high-speed, high-performance devices.

Higher I/O density. Redistribution layers serve as a rerouting of the I/O layout and enable a higher I/O count. A high I/O density generally begets better electrical performance, as more outputs results in faster electrical signals between die and minimizes the risk posed by electrical shorts. A higher I/O density also enables the package to perform more operations in parallel. Therefore, a high I/O count allows for more complex, high-speed die to be packaged.

As previously mentioned, in FOWLP the bumping is not dependent on the die surface and therefore a higher I/O density can be achieved by fanning out the electrical interconnections with the implementation of more RDLs. In the most advanced fan-out packages, up to four RDLs may be used for the purpose of maximizing I/O density, which in turn facilitates improved electrical and thermal performance, including power dissipation. In the case of TSMC's InFO, a 10% improvement in power dissipation is achieved using fan-out packaging [5].

More functionality. Smarter phones deliver more functions for the user, through greater memory storage, more sophisticated cameras, faster WiFi®, touch screens, voice recognition, high-performance CPUs, longer battery life, and motion sensors that are essential for mobile gaming. The trend, however, is towards thin phones, which poses a challenge for IC and packaging manufacturers: how to fit more functionality into slim smartphones? The answer is integration, and there are various ways to

achieve this using fan-out packaging.

Both heterogeneous and homogeneous integration are achieved by embedding more ICs and passives within the same package and also by utilizing more complex packaging architectures. One example is the multi-chip package, wherein multiple dies of various functionalities are embedded into a mold compound within the same package. Another way to achieve more integration and functionality is to use a package-on-package, such as TSMC's reputable InFO package (DRAM on APE) which is used in the latest iPhone models [6]. There are numerous other fan-out packaging technologies that employ 2D, 2.5D, or 3D architectures in order to maximize integration; i.e., system-in-package (SiP), multi-chip module (MCM), and stacked dies, among others.

Smaller form factor. The aforementioned drivers – performance and functionality – are directly correlated to another key driver: smaller form factor. Manufacturers are tasked with building next-generation smartphones, with better performance and more functionality than their mobile predecessors, while not compromising the sleek and slim design that consumers so fervently demand. Therefore, next-generation smartphones require denser packages, which are made possible by transistor scaling (Moore's Law) or advanced integration using innovative packaging technologies.

Through implementation of die embedding, in combination with the fine-feature processes possible with wafer processing, FOWLP minimizes the number of RDLs required to form a high-density package while not suffering from excessive cost penalties. As the RDL can be formed across the whole over-mold area, it is possible to eliminate the need for an IC substrate or interposer altogether, which decreases the form factor considerably over traditional packaging techniques.

With integration, and specifically, by embedding multiple die within the same package and with use of innovative packaging architectures, form factor can be reduced even further. According to C. C. Wei, co-CEO at TSMC, InFO technology enables a twenty percent reduction in package thickness [5]. Meanwhile, Yole Développement has estimated that the form factor reduction provided by fan-out packaging is at least 40% compared with standard flip-chip packaging [3]. Flip-chip, currently the more prevalent packaging technology in high-volume production, requires an IC substrate that results in a

larger form factor and footprint than that of FOWLP. The use of a multilayer substrate in flip-chip packages also contributes significantly to the overall manufacturing costs when compared to FOWLP, which uses a low-cost mold material.

The technical benefits of FOWLP are numerous, substantiated, and increasingly difficult to ignore: 1) better reliability performance by means of embedding and more RDLs; 2) more functionality and higher levels of integration through multi-chip embedding and complex architectures; 3) form factor reduction via innovative architectures; and 4) substrate-less embedding technologies for reduced manufacturing costs. For these reasons, the semiconductor industry will witness the substantial and widespread adoption of FOWLP technologies in the coming years.

Fan-out: exponential growth

Frequently described as a disruptive technology, fan-out will change the packaging landscape with further adoption by outsourced semiconductor assembly and test suppliers (OSATS), integrated device manufacturers (IDMs), and foundries alike. Fan-out packaging, while having recently gained momentum with the entrance of TSMC's InFO, is not a new technology, however. Embedded wafer-level ball grid array (eWLB) is a type of fan-out packaging that has been in production at Infineon for nearly a decade [7]. Variations of Infineon's second-generation eWLB technology have been co-developed, qualified, and/or licensed by companies such as STMicroelectronics, STATS ChipPAC [8], NANIUM S.A., and ASE [2]. Other types of fan-out packages are being produced in low volume at Nepes and Deca Technologies [2].

TSMC's entry with its innovative InFO technology has, and will continue to have, a far reaching and lasting impact on the fan-out market. If Apple continues to use InFO PoP technology in future generation iPhones, surely there will be followers.

In absolute numbers, the expected growth in fan-out technologies will be exponential, going from \$244M in 2015 to \$492M in 2016, and sprouting up to \$891M in 2017 [2]. According to [2], the forecast for 2021 is a remarkable \$1.3B with substantial growth in both the eWLB and PoP market segments. Market reports by JMS [1], TechSearch International [9], and Prismark [6] similarly forecast substantial growth for fan-out packaging.

Fan-out: key challenges

The technical advantages and the forecasted market growth, position fan-out as the preferred advanced packaging technology for next-generation mobile devices. However, there are several process challenges associated with fan-out packaging: warpage, die shift, yield, and the transition to panel-based manufacturing [2].

Warpage is a critical processing challenge for fan-out based technologies. When thinner packages are used, in addition to heterogeneous materials and more Cu layers (RDLs), wafer bowing occurs after processing. Wafer bowing is a result of unequal stress distribution over the wafer and influences yield. To overcome this, manufacturers must optimize their process sequence and fan-out design [10].

Die shift is another process challenge and is a result of the slight movement of the die, after placement on the carrier wafer and during the over-molding process. Die shift is a challenge for wafer-based technologies, however, with the desired migration to panel formats, die shift becomes even more critical, as the equipment to handle the consistent and accurate die positioning on a large square format are simply not yet proven. Die shift impacts yield, which is one of the primary concerns for both wafer- and panel-based fan-out packaging.

Qualcomm has stated that a 300mm wafer produces approximately 616 packages, compared to 1,911 from an 18 x 24 inch panel (10 x 10mm package size) [3]. Therefore, a transition to panel-based fan-out packaging would enable significant cost savings for manufacturers, but only if the infrastructure is available and capable. Unfortunately, existing panel-based PCB equipment is not prepared to successfully address the requirements for miniaturization, RDL pitch down to 2 x 2µm, as the tools are not designed for such fine dimensions. This is one of the many reasons why a direct transfer is not currently possible onto standard PCB equipment. Equipment manufacturers and material suppliers are also not currently able to offer solutions for overcoming panel warpage and die shift. Finally, standardization is also a challenge, as PCB manufacturers utilize a wide array of panel sizes.

Fan-out: Cu plating application requirements

The following sections discuss requirements for Cu plating applications relative to fan-out packaging technologies.

Requirements for RDL. Trends for next-generation mobile devices – thinner smartphones with more functionality – require miniaturization at all levels. For advanced packaging technologies, miniaturization involves decreasing the RDL pitch down to 2 x 2µm and below. Redistribution layers are essential to fan-out technologies, as it is with more RDLs that I/O density is increased. Successful formation and plating of such fine features pose a challenge for both suppliers and manufacturers, with the plating challenge being the simultaneous plating of fine lines and spaces (2 x 2µm), large Cu pads (up to 300µm), and in some cases also microvias (example: 5 x 10µm) with a deposition rate that optimizes throughput.

Requirements for Cu pillar. Cu pillars are needed for certain types of fan-out packaging such as package-on-package (PoP), in various dimensions including both standard pillar in the range of 40 x 50µm and tall pillar in the range of 200 x 50µm. The standard performance requirements – high-throughput, high-yield, and optimal reliability performance – can be met with an optimized Cu pillar process that enables uniform and pure Cu deposition using high-speed plating. High-speed plating will result in a higher throughput, however it also increases the risk of voiding in the intermetallic phase of Cu and SnAg (**Figure 3**) and influences uniformity, both of which impact the electrical performance and yield. The purity of the deposit, and specifically the presence of organic co-deposition, also influences the voiding performance. Therefore, a good Cu pillar process should enable high-speed plating of pure and uniform Cu. This can be achieved with the right organic additives and high-speed plating equipment that collectively reduce the occurrence of organic co-deposition and optimize uniformity.

When electroplating tall Cu pillars, the situation becomes more complex, as high aspect ratio structures are more difficult to plate in a timely manner. Structures with a 1:1 aspect ratio (AR)

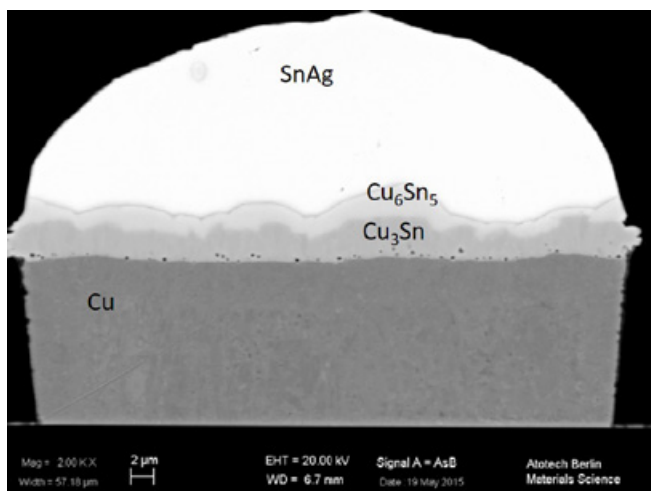


Figure 3: The image shows void formation in the intermetallic phase between Cu and SnAg. The voids appear as small black spots.

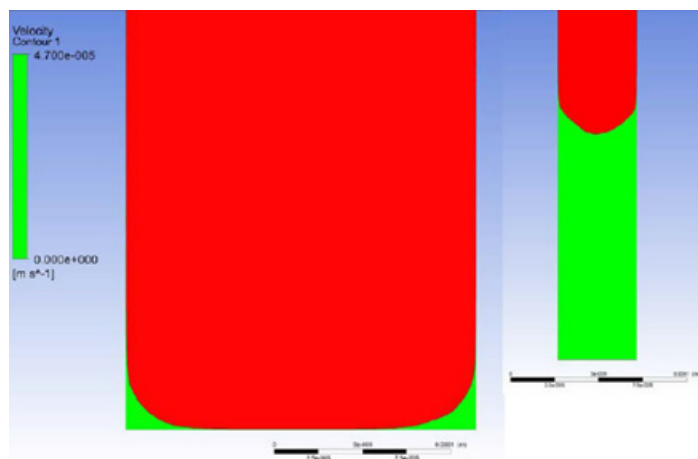


Figure 4: The diagram illustrates the prevalence of diffusion speed (green), in comparison to convection (red), for high aspect ratio (HAR) pillars. The approximate ARs are 1:1 (left) and 4:1 (right).

are efficiently plated with primarily convection-controlled plating, however structures with ARs up to 4:1 involve a different plating mechanism (**Figure 4**).

During plating of high AR structures, mass transfer via diffusion occurs at the pillar base, while fluid exchange via convection takes place at the top of the

pillar structure. As the diffusion layer thickness increases, the limiting current density decreases, making it more difficult to achieve a rapid deposition speed at the bottom of a high AR structure. Therefore, for fast plating of high AR structures, the diffusion layer thickness should be controlled.

For plating low AR (1:1) structures, convection supports fast plating, and therefore the electroplating equipment has the primary role of facilitating deposition. Electroplating equipment with systems and features that enable optimum and direct electrolyte flow and programmable agitation enable high-current density



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plating, and when coupled with the right organic additives and reverse pulse plating capability, will support optimized uniformity and limit organic co-deposition, to produce a pure Cu deposit.

Electrolyte flow, agitation, and the additives, however, have limited influence on diffusion-controlled mass transfer or its limiting current density. Plating beyond 90% of the limited current density will result in dendrite formations in the Cu grains, as shown in **Figure 5**. Excessive dendrite



Figure 5: An example of dendrite formations in a Cu deposit.

growth hinders soldering, causes shorts between Cu RDL lines when plating RDLs, and negatively impacts reliability. Therefore, for high-speed plating of high AR pillars, the limiting current density must be increased. To increase the absolute value of the current density in the bottom of the pillar structure, where diffusion occurs, certain process parameters may be modified. Temperature and the Cu content of the electrolyte should be increased, and acid concentration must be optimized.

In summary, the applicable current density that can be applied for defect-free plating of high AR pillars is lower than that for plating structures with dimensions similar to standard pillars (40 x 50µm), resulting in a longer plating time and consequently lower throughput. To achieve defect-free and high-speed plating of tall Cu pillars, the right organic additives and high-speed plating equipment are needed, as well as a process that optimizes temperature, the Cu electrolyte content, and the acid concentration.

A turnkey solution for Cu plating in fan-out packaging

Atotech offers a turnkey plating solution (chemistry and equipment) that

satisfies all aforementioned requirements for RDLs and both standard and tall Cu pillars. In addition, we offer a chemistry-only Cu plating process for plating RDLs and pillars.

Spherolyte Cu process. Our Spherolyte process includes high-purity chemistries and organic additives for Cu plating. We have a specially designed Cu RDL and pillar plating process for use in a newly developed equipment (MultiPlate) for very high-speed plating, as well as standard electrochemical deposition (ECD) plating equipment. Both processes satisfy all aforementioned requirements for the Cu deposit while providing a high deposition rate [11].

MultiPlate. Our MultiPlate is an ECD plating tool for very fast deposition of Cu. It is equipped with technical features that enable optimal electrolyte flow, programmable agitation, and reverse pulse plating at very high-current densities. To date, plating results generated in this tool demonstrate a better performance, in terms of deposition rate, uniformity, and the purity of the Cu deposit, than industry standard Cu plating solutions. When plating very thick Cu, as in the case of tall Cu pillars, the advantage of very high-speed plating is even more substantial.

The technical benefits of MultiPlate's key features [12] include: 1) advanced fluid delivery; 2) segmented anodes that enable adjustable current distribution by segmentation for optimized uniformity; 3) free programmable agitation that allows for the precise movement of the substrate for optimized agitation and flow; and 4) pulse reverse plating that enables the control and stabilization of the Cu pillar plating performance with physical parameters, thereby eliminating the need for a leveling additive.

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Biography

Cassandra Melvin received her BS in Business Management at Rensselaer Polytechnic Institute and is Global Product Manager for Advanced Packaging at Atotech Deutschland GmbH; email Cassandra.Melvin@atotech.com

Roger Massey received his BS in Materials Engineering from Sheffield Hallam U. and is Technology and Strategic Marketing Manager for Atotech Deutschland GmbH.