Next-generation copper pillar plating technologies

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As the industry moves towards smaller, faster devices, there is mounting pressure on all members of the supply chain to enable higher performance at lower cost. The limitations of Moore's Law are becoming more evident as advanced technology nodes are no longer providing a significant cost benefit. R&D investments in next-generation sub-10nm node lithography tools are becoming increasingly expensive and perhaps are no longer the viable solution for improving cost effectiveness. As a result, the industry has shifted its focus to advanced packaging as a means for providing better performance and lowering costs, following the so-called "More than Moore" approach. There are three primary drivers for this shift: improved performance, more functionality, and cost reduction. This article will discuss how these three drivers have led to the emergence of flip-chip packaging using pillars and the current and future challenges for Cu pillar technology.

Various packaging technologies have been tested for their ability to provide substantial technical advantages while reducing the overall production flow and minimizing manufacturing costs. Currently, the preferred packaging technology for sub-45nm node technologies is flip-chip because of its ability to offer a significantly improved I/O density and minimized footprint compared to standard wire bonding, as well as better thermal and electrical performance. Flip-chip technology is relatively inexpensive compared to other emerging packaging technologies and currently accounts for approximately 16% of the 200mm packaging market, according to industry reports. Many of the key players in the packaging industry already utilize flip-chip in high-volume manufacturing and the five-year forecast is promising, showing steady growth for flip-chip across all market segments with the most substantial growth in the consumer electronics sector.

During the flip-chip process, the die is flipped over and connected to the substrate prior to being packaged. Connection is possible by various applications but the primary two are soldering or using pillars. Flip-chip ball grid array (BGA), which used SnAg solder balls to connect the chip to the substrate, has been the preferred method in the past but is slowly being surpassed by Cu pillar. The two methods of soldering, paste printing and micro ball placement, have their own set of limitations, namely the resolution of the printing equipment and the slow and costly micro ball placement process. For the most advanced technology nodes, Cu pillar is the preferred application for the first layer interconnect process and will account for the majority of future growth in the flip-chip market segment.

Copper pillar plating process and requirements

During the plating process, the die is connected to the IC package by two layers of Cu pillars – the first layer interconnect on the die side and the second layer interconnect on the substrate side. To further increase the I/O count, an optional redistribution layer (RDL) may be plated on the die side. The Cu pillar is electrolytically plated according to the application requirements for height and diameter, usually followed by a thin Ni diffusion barrier (up to 3µm), and finally a Sn or SnAg cap.

The critical requirements for pillar plating – high throughput, exceptional reliability performance, and high yield – can be optimized using a high-speed plating process that can achieve superior uniformity and voiding performance.

Throughput is directly correlated to the deposition speed (as well as the design of the plating tool) and therefore, applying higher current densities will, in most cases, result in an increased throughput. High-speed pillar plating, however, generally has a negative impact on the voiding performance and uniformity. Excess voiding is a common problem when plating at higher current densities and especially in the absence of a Ni diffusion barrier on top of the Cu. Furthermore, using standard Cu plating chemistries and while plating at current densities of 10+ ampere per square decimeter (ASD) it is difficult to satisfy the industry's requirements of <5% for nonuniformity. Both voiding and nonuniformity impact the electrical performance, which is a measure of reliability, as well as the yield.

Furthermore, the purity of the bath – and specifically the level of additive incorporation – has a direct impact on the voiding performance, as a less pure or "dirty" plating bath with significant additive incorporation results in more voids. This problem can be overcome by optimizing the additive suite utilized during the plating process. Typically, three additive suites are used in Cu plating, including accelerators, which selectively speed up the deposition, suppressors that selectively slow the deposition, and levelers that support a uniform thickness distribution.

The plating mechanism at work is determined by the additive suite and contributes to the voiding performance and uniformity of the deposited Cu. The plating chemistries, therefore, are what determine how the plating process will perform and impact throughput, reliability, and yield, as well as the quality of the deposited Cu. Therefore throughput, reliability and yield can be optimized by improving the existing plating chemistries so that uniformity and voiding performance

are not compromised with higher current density plating.

For future requirements of even higher throughput – and therefore significantly faster deposition rates along with further improved yield – completely new technologies are needed. Standard electrochemical deposition (ECD) tools and chemistries will reach their technical limitations, so new solutions with vastly different technologies must be developed to enable high-speed pillar plating with the best reliability performance.

To address the current and future process requirements for pillar plating, we have expanded our semiconductor product portfolio with the next-generation of Spherolyte Cu pillar plating chemistries, as well as an electrochemical deposition tool designed for high-speed pillar plating. The next sections will highlight the performance of these new technologies compared to their previous, industry accepted pillar plating process.

Spherolyte RDL/pillar UF2 and UF3 processes

As throughput is directly correlated to deposition speed, the development of new electrolytes with faster deposition rates is paramount to satisfying the industry requirements for high throughput. The improvement of the Cu deposition rate beyond the industry standard of 1-2µm/min is critical for next-generation packaging technologies; however, uniformity must not be compromised as a consequence. Uniformity of Cu pillars is a prerequisite for a regular soldering process without any opens between the pillar on the die and its counterpart on the IC substrate. Usually, uniformities, or to be precise, nonuniformities are calculated and expressed as shown in **Figure 1**. Most pillar plating applications require a nonuniformity rate of 5% for within-wafer (WIW) and within-die (WID), with a profile (WIP) variation of less than 2µm.

Key to the development of a new additive suite is the leveler. This is a specific N-containing additive molecule that interacts with the other additives, namely the accelerators, usually SPS, Bis-(sodium sulfopropyl)-disulfide containing. The combination of accelerator and SPS controls the property of the Cu deposit, including: 1) Physical properties like hardness, resistivity, etc.; 2) Grain size; 3) Roughness; and 4) Uniformity and profile.

Profile and uniformity are linked to each other. Profile requirements may vary according to the specific application requirements for shape and form. Standard pillars are rectangular in shape, however oval and rounded pillars are not uncommon, and some pillars are placed on top of a recess structure known as pillar on pad. Therefore, different electrolyte systems are needed to comply with the varying requirements.

High-speed systems for conformal plating

The first electrolytic system to be discussed is the second-generation of electrolytes for Cu pillar plating. It is a purely conformal plating process, meaning that the Cu deposition exactly follows the given underlying shape, i.e., a flat surface will result in a flat Cu surface and a waved surface will result in a waved Cu surface. The benefit of such an electrolyte system is that Cu deposits are usually perfectly flat and smooth as long as the underlying pad structure is as well. In this case, the pillar shapes are flat without any doming or dishing (see **Figure 2a**). This example has been plated with Spherolyte RDL/pillar UF2 at 3.8µm/min. These electrolytes can be used for much higher deposition speeds, up to 4.4µm/min, as shown in **Table 1**. It should be noted that the uniformity is also a function of the layout. Generally, standard layouts can be plated with higher current densities.

Limitations of conformal plating

While the ability to create a perfectly flat (uniform) pillar shape is advantageous, it also has limited use for pillar in pad applications, wherein the Cu pillars are built on top of a µ-via as shown in **Figure 3b**.

The remaining recess after plating

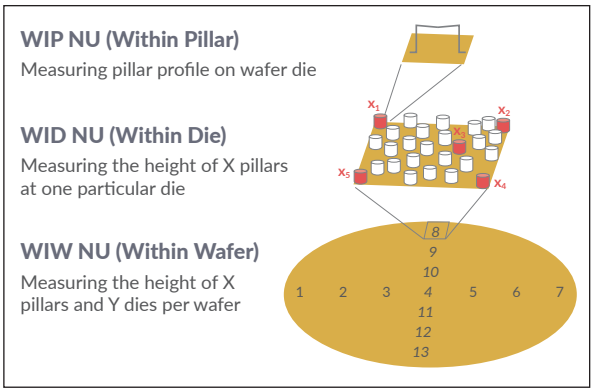

Figure 1: Nonuniformity calculations for Cu pillar plating. The example shown is for WIW with 13 dies.

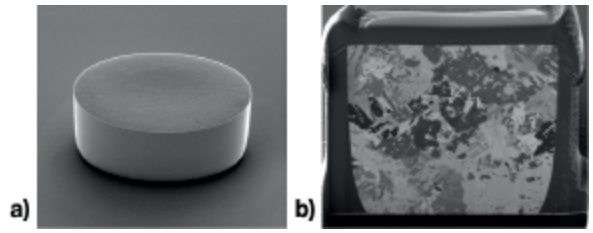

Figure 2: a) (left) Example of a 20µm oval Cu pillar plated with a conformally deposited electrolyte at 3.8µm/min. b) (right) An FIB cut through the Cu pillar.

Speed	3.3 µm/min	3.9 µm/min	4.4 µm/min
Non uniformity	15 ASD	17.5 ASD	20 ASD
WIW	2.5 %	3.0 %	4.6 %
WID	2.2 %	2.4 %	4.5 %
Profile	1.5 %	1.7 %	2.3 %

$$Non-uniformity\ \% = 100\ \% \frac{(Zmax - Zmin)}{2\ Zave}$$

Table 1: Example of nonuniform plated Cu pillars at different deposition speeds using the Spherolyte RDL/pillar UF2 process. Numbers given are for test wafers plated in a fountain type plater. The pillar height is 27µm in a 42µm thick resist.

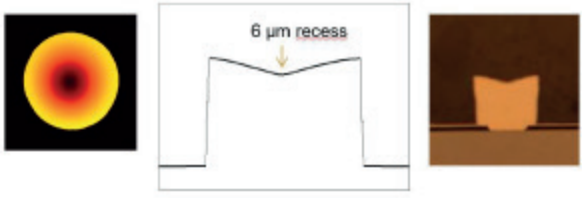

Figure 3: A Cu pillar plated on top of a µ-via with a conformally plated electrolyte (Spherolyte RDL/pillar UF2) with a pillar height of 45µm and a pillar diameter of 55µm.

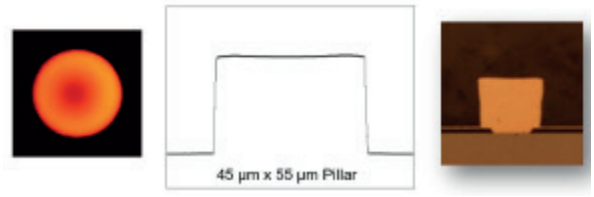

Figure 4: The same Cu pillar type (over µ-via) as in **Figure 3**, plated with a new generation of electrolyte (Spherolyte RDL/ Pillar UF3). The pillar height is 45µm, and the diameter is 55µm. The plating was at a deposition speed of 3.3µm/min with a 1µm recess. Within-die and within-wafer nonuniformity are <3%.

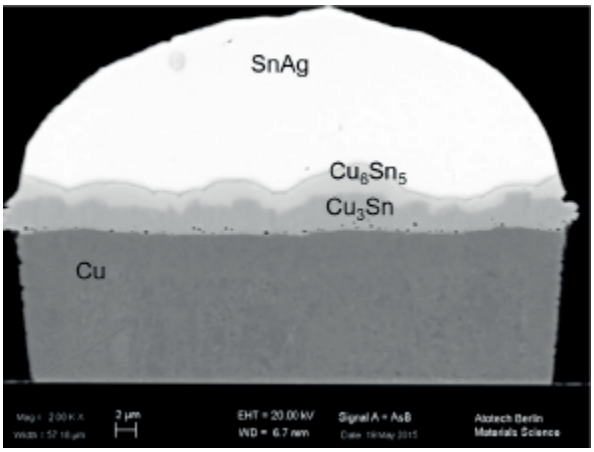

Figure 5: Void formation in the intermetallic phase between Cu and SnAg. Voids appear as small black spots.

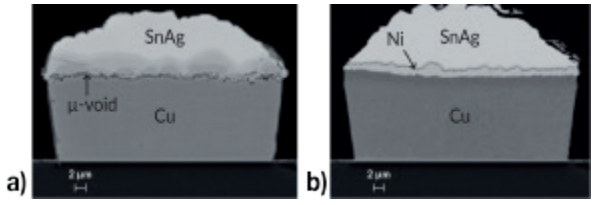

Figure 6: Example of void appearance and its suppression: a) (left) Void formation for a Cu-Sn interface after 250 hours of storage at 150°C; a chain of voids is visible; b) (right) There are no voids for the same Cu pillar with a 3µm Ni diffusion barrier between 20µm Cu and 15µm SnAg. Plated in in Fountain type plater at a deposition rate of 2.2µm/minute.

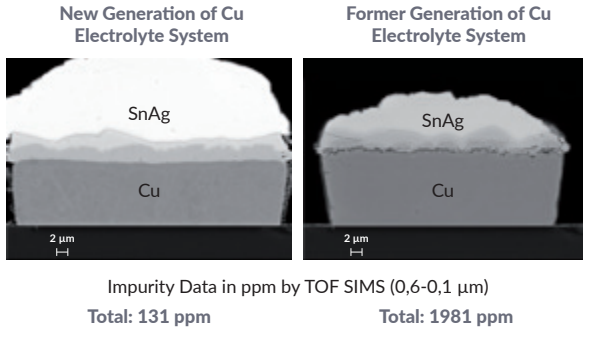

Figure 7: Cu-SnAg pillars after 250 hours of storage at 150°C: a) (left) The resulting pillar plated with the latest generation of Cu pillar electrolytes (Spherolyte RDL/pillar UF3) in a fountain plater without an intermediate Ni barrier; b) (right) The reference system is the Spherolyte RDL/pillar UF2. Both samples were plated at 2.2µm/min in a fountain plater.

such pillar types usually mirrors the exact depth of the µ-via underneath. Such recesses can be used for placing solder material on top of the pillar, however, most packaging companies prefer perfectly flat surfaces. This in turn requires a completely different additive system, one with a different filling capability.

Copper pillar plating for pillar in pad apps

Next-generation electrolytic systems are comprised of altogether different additives. The main role of these additives is to level out every recess while maintaining a flat surface on flat wafers (**Figure 4**). This requirement is a contradiction in itself for an electrolytic system. Therefore, these additives systems do not give perfectly flat pillar surfaces on flat substrates but rather slightly convex-shaped pillars. Nevertheless, the degree of this convex shape needs to be in-line with the usual requirement of 5% nonuniformity.

Voiding in the intermetallic phases

It is a well-known fact that intermetallic phases between solder and Cu are prone to void formation [1,3]. These voids appear only after a certain heat treatment (reflow), and not directly after plating. An example for such a void formation is given in **Figure 5**.

The voids (black spots in **Figure 5**) appear after storing the wafer at 150˚C for 250 hours, predominantly in the Cu-rich intermetallic Cu_3Sn. Voids appear both with SnAg and Sn solders on Cu pillars. According to [1], such voids are caused by the electrolyte system itself, mainly by a complex formed out of leveler and accelerator (SPS) in the Cu process. Some accelerator/leveler complexes are significantly incorporated during the plating process and can lead to small crystallization failures. Cu and Sn are known to interdiffuse quickly into each other and so do the crystallization failures. The latter can accumulate at the boundary of Cu and Cu_3Sn. Severe voiding can lead to disintegration of the solder joint and result in electrical failures.

One strategy to avoid such voids is the use of a diffusion barrier between Cu and Sn, while another option is to use modified electrolyte additives that are less incorporated. The industry standard is to plate a thin Ni layer as a diffusion barrier. **Figure 6** shows the interface of such a metal stack (Cu-Ni-Sn) after heat treatment. There are no voids visible. The main disadvantages when using a Ni diffusion barrier are the additional process steps and the blocking of plating cells in the single-wafer tools, thereby reducing the overall throughput of the tools.

The new generation of Cu additives overcome the problem discussed above. These electrolytes show significantly reduced incorporation levels of additives into the plating bath. This has been proven by secondary ion mass spectrometry (SIMS). **Figure 7** compares the new generation of Cu pillar additives with the older generation. The resulting SIMS data show that the amount of examined incorporated impurities in the Cu pillar is significantly reduced. Impurities have been measured in a layer thickness of 0.6-1.0µm. As a consequence, the level of void formation is reduced to an acceptable amount.

A new solution for copper pillar plating

The Spherolyte RDL/Pillar UF3 process is a solution that satisfies all performance requirements for Cu pillar plating. The main features of our new process are a pure Cu deposit due to low incorporation of additives, a nonuniformity of <5%, no voiding in the intermetallic phase prior to

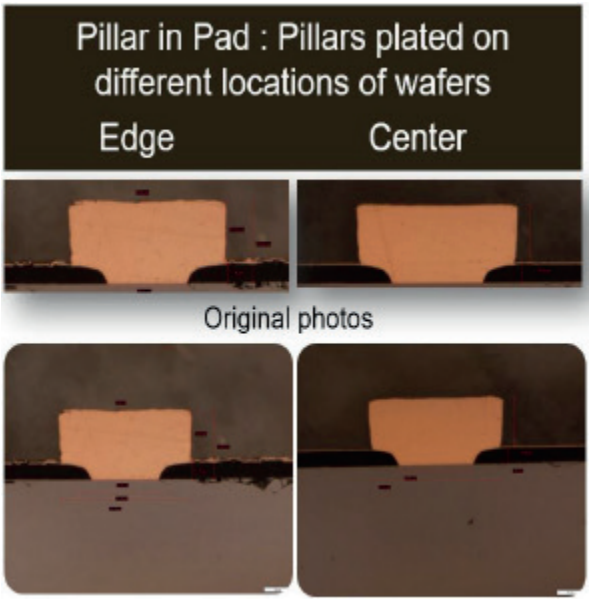

Figure 8: Cu pillar in pad technology.

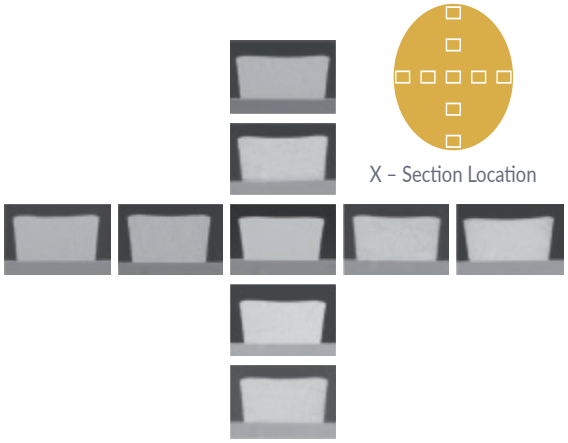

Figure 9: Example of profile uniformity of Cu pillars plated with Spherolyte chemistries at 20 ASD on MultiPlate. The cross sections were taken at nine different locations on a 300mm wafer.

reflow, faster plating at 15+ ASD (up to 4.4µm/min), and the elimination of the Ni diffusion barrier typically required to prohibit migration and voiding in the intermetallic phase. Additionally, this next-generation electrolyte system is suitable for both standard pillar plating, as well as pillar in pad applications (Figure 8). Using this new process, plating of Cu pillar in pads is optimized and dishing is minimized.

A new technology for high-speed pillar plating

While the new Cu electrolyte system has shown satisfactory results at standard current densities, as requirements for high-speed pillar plating go well beyond 10 ASD, new technologies must be considered for optimal plating performance. In order to achieve successful plating at very high current densities (20+ ASD), completely new technologies are needed as the chemistries alone are no longer capable of optimum performance on standard fountain plating tools. Therefore, there is a need for new equipment that is capable of high-speed pillar plating at 20 ASD and beyond. The requirements for a tool capable of 20+ ASD must include systems and mechanisms for enabling optimized uniformity, low impurity incorporation and therefore, void-free plating, and highest possible throughput.

Our solution for enabling high-speed pillar plating is MultiPlate (Figure 9)—a tool for electrochemical deposition in advanced packaging technologies.

Solutions for enhanced uniformity

The new system utilizes a reverse pulse system for optimal uniformity (no doming or dishing) in high-speed pillar plating, made possible by an integrated multipurpose rectifier. A copper dissolving unit is implemented for monitoring and replenishing the Cu concentration via an external unit. This has a direct impact on the additive incorporation and purity of the bath, and therefore the uniformity and voiding performance of the deposited Cu.

Dimensionally stable inert anodes are used in a segmented design with two and three segments for 150, 200 and 300mm wafers or panels, respectively. The segmented anodes enable an adjustable current distribution throughout the entire wafer surface, allowing an optimized within-wafer uniformity. An advanced fluid system is used for optimizing electrolyte flow distribution by means of a short distance from the cathode (wafer) to the segmented anode. This provides a direct flow to the wafer and improved agitation, both of which are required for high-speed pillar plating and a uniform thickness distribution.

And finally, a free programmable mechanical agitation mechanism enables the movement of the wafer holder within a mere 35mm from anode to cathode, thereby eliminating the risk of spray and flow patterns and consequently improving the overall uniformity.

Summary

In summary, the Spherolyte UF3 process fulfills all requirements for Cu pillar plating; pure Cu is deposited using a high-speed pillar plating process, without compromising the voiding performance or uniformity. For next-generation requirements for pillar plating, at current densities beyond 15 ASD, MultiPlate is a solution for optimized performance; high-current density plating of pure Cu, with improved uniformity and voiding performance.

References

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Biographies

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