Upscaling panel size for Cu plating on FOPLP (Fan Out Panel Level Packaging) applications to reduce manufacturing cost

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Abstract

Electrolytic metal deposition is a key process step in the manufacturing of vertical and horizontal interconnections used in today's PCBs and IC substrates on one hand and advanced packaging applications on the other hand. Historically both application areas were clearly defined and separated by different requirements in feature sizes and substrate formats. PCBs and IC substrates were based on organic large scale substrates with rather large features while advanced packaging technology is wafer based with the capability to incorporate fine features down to a few microns.

The ever increasing demand of higher performance, lower cost and thinner end user devices like smartphones require intense developments and innovation in all areas of the electronic component design including the substrate and chip packaging. Latest manufacturing technologies in both areas like fan-out wafer level packaging and advanced substrates are constantly emerging and promise to be a critical piece to meet these requirements. As a consequence both areas are currently merging while creating a new application segment. This segment combines the request of small feature sizes with the manufacturability on large scale substrates. Obviously many of the traditional process technologies like plating and available equipment cannot be easily adopted and need certain developments, adaptions and improvements.

In this respect, a key challenge in the area of electrolytic metal deposition is the combination of various challenging requirements: creation of feature sizes down to 2µm L/S with heterogeneous feature density on large substrates up to 600mm at excellent metal thickness uniformity and high plating speed. The paper presents latest studies and conclusions in critical performance areas of the plating process such as electrolyte fluid dynamics, impact of anode design, pulse reverse rectification and newly designed electrolytes. Finally latest test results of optimized process conditions will be discussed in detail with different feature sizes providing data of within die and within substrate uniformity. All tests are done on panel level, both organic and glass substrates.

The latest findings and achievements of the discussed panel based plating process technology will support the industry to develop panel based packaging processes that meet both technical and commercial requirements.

Key words

FO-PLP, RDL, advanced packaging.

I. Introduction

The number of connected devices is growing fast (from 25 billion today up to 100+ billion in 2050) and the devices are becoming much smarter. This means we will need more complex devices utilizing the same real estate and lower costs. Years ago Fan-Out Wafer Level Packaging (FO-WLP) has been introduced and is now seen as a key technology to meet future packaging requirements of the industry. Now the industry is interested to increase the through-put and lower the total cost by increasing the substrate sizes even larger than the commonly used printed circuit boards (PCB) panel formats like 510 × 515 mm² or 458 × 610 mm².

The idea of substrate manufacturers is to use the existing infrastructure and experience in handling of square formats to keep the costs low. However adjustments have to be made for handling and processing of these formats while meeting the requirement of excellent surface distribution to meet the yield targets. The biggest savings will only come from batch activities. During production of a Fan-out package, RDL creation is considered to have the largest impact by approx. 40% of the overall costs [1]. The largest portions of the RDL cost itself are material cost like photo-dielectrics and plated Cu and equipment related costs for patterning and metallization. Material costs are expected to remain on a similar level, whereas equipment costs per package directly relate to the number of packages per substrate that can be processed with a single process step.

In this paper we are describing the concept of a plating tool called MultiPlate®. Based on years of in-house experience this tool was introduced for fabrication of wafers in 2013 and for panel formats up to 510 × 515 mm² in 2016. This year the latest version was installed for detailed investigations, allowing for processing of panel sizes up to 650 × 600 mm. The concept is to provide a tool that improves the technical performance of the process step manufactured on a much larger substrate combined with cost efficient equipment solutions, keeping the output in substrates per hour at a minimized equipment cost increase per panel. Key challenges, latest technology developments and test results on panel level will be presented in the following sections.

II. Technology Challenges for Panel Plating

A. Challenges for Plating Process

During copper electro-plating the metal is deposited into a mold of thick photoresist or photo definable dielectric material on top of a seed layer. The structures to be plated can be a large connection pad (up to 250-350 µm) or so-called µVias with sizes of e.g. 10×15µm to connect different layers and as well redistribution layers (RDL) of different sizes. Nowadays typical sizes of RDL traces in a Fan-Out package design are in the range of 8-10 µm, the roadmaps ask for resolution down to 2-5 µm. The key challenge for the plating process is to deliver very uniform Cu deposition across a single layer that includes a wide range of different structures. Different feature sizes and different required Cu thicknesses play a very dominant role to the plating result.

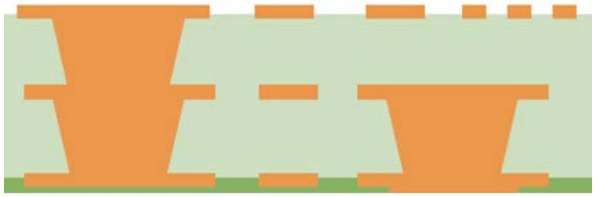

Figure 1. Schematic illustration of Cu plated features in a dual RDL package design, including µVias, RDL traces and Cu pads.

For interconnecting the stacked chips, the package-on-package (PoP) technology uses Cu pillar plating in various dimensions: standard pillars in the range of 40 × 50 µm as well as tall pillars with heights of up to 200 µm [2] are required to connect the different chips. Figure 2 gives an example of the wide variety of required plated Cu features in a leading edge FO-WLP design.

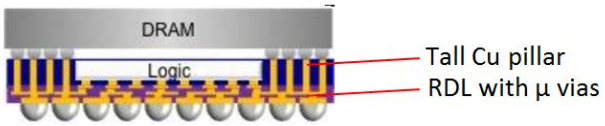

Figure 2. FO-P Package-on-Package example for advanced processor application with tall Cu pillar, RDL and µvia structures [3].

The optimal copper plating process needs to enable high throughput, high yield and optimal reliability. During plating it is critical to ensure high purity deposition of copper, as it influences the voiding performance and physical properties of the deposition. One of the challenges of moving to panel processing is to keep similar deposition performance achieved on wafer level and transfer it to the much larger surface at no compromise.

To meet the different technology requirements, we have developed specific processes for Cu RDL and pillar plating consisting of high-purity organic additives. The new Innolyte® electrolyte is designed for use in a dedicated panel plating equipment designed for very high-speed plating. The combination of process and equipment is key to satisfy the technology needs by providing a high deposition rate while with achieving the requirements for

the Cu deposit.

B. Challenges for Plating Equipment

The emerging market of FO-PLP consists of a diverse array of substrate materials and sizes as the industry seeks to adapt each participants, particular supply chain and expertise. The result for the equipment supplier is a new market that requires customized solutions to support each player. These customized solutions include: covering the individual process modules as well as the related substrate handling systems & components. Technology wise, the panel distribution is mainly influenced by equipment features and increasing the size and changing the shape of the substrates need optimisation of tank design as well as design of the panel holder system. The challenge for the equipment supplier is to minimize the equipment costs for different manufacturer panel sizes while providing an excellent plating environment to deliver an attractive cost-of-ownership (CoO) to support both FO-PLP development and adoption of the production process.

III. Technology Suite for Panel Plating Processing in FO-PLP

The unique approach to panel level plating for FO-PLP involves taking many of Atotech's core competencies and applying them to this new emerging market. The approach involves both plating process equipment (including chemical additives) and substrate handling technologies as a complete system solution. Continuous development is ongoing as electrolytes are tailored specifically for vertical plating targeting the specific demands of FO-PLP products. Likewise, equipment development is realized in concert to achieve the physical parameters required to support the overall process requirements and targets. New substrate handling systems are meeting the substrate requirements considering the various geometric considerations of size, material and warpage.

A. Electrolyte and Process

There are two major applications of panel level packaging and for each, a specific electrolyte was developed. On the one hand there is a two additive electrolyte for tall pillar plating, with the major focus of high applicable current densities of about 20 ASD (A/dm²), rectangular pillar shape and very good with-in-unit and with-in-panel uniformity. On the other hand there is the development of an RDL plating electrolyte focusing on within-unit distribution and filling at current densities higher than 4 ASD. It has to be considered that there are various features to be plated in RDL plating (e.g. fine lines down to 1-2 µm lines and spaces in combination with pads & mass plane areas at the same time) and depending on the application there are blind micro vias, that need to be filled, with a relatively low surface copper thickness of around 2-10 µm. To fulfil these challenging requirements, a three additive system is needed, where the concentration of each additive can be adjusted individually. In both cases RDL & tall pillar plating, there is an advantage to use pulse plating, which improves distribution & feature shape in RDL plating and allows to use higher current densities and improves the pillar shape in tall pillar plating as well. A well-established plating technology to apply pulse reverse plating without the risk of creating surface defects is the use of a Fe^{2+} /Fe^{3+} redox system. The combination of reverse pulse plating, iron redox plating system and the additives choices for RDL and tall pillar plating helps to achieve the future requirements for the PLP market. The summary of additives & current plating requirements for FO PLP applications is shown in the table 1 below.

Table 1. Additives & current plating requirements

Application	Products	Dimensions	Target CD
RDL-Plating	**3 additive system** EXPT Innolyte PLP Accelerator EXPT Innolyte PLP Suppressor EXPT Innolyte PLP Leveller	L/S: 5/5 µm (future 2/2 µm and below) BMVs: 15 × 10 µm (dia x depth, smaller in future)	CD ≥ 4 ASD
Tall Pillar Plating	**2 additive system** EXPT Innolyte P Accelerator EXPT Innolyte P Leveller	Pillars: 200 × 200 µm (dia x depth; future 50 × 200 µm)	CD ≥ 20 ASD

The With-In-Panel Distribution=WIPD is calculated as follows: WIPU= ± max-min/2×mean × 100% and here the target is to be better than ±10 %. However, the development goal is to be better than ± 5 %.

B. New Developments for Equipment

Latest equipment developments can be grouped into 3 subsets: pre-wet process cells, plating cell system and substrate handling.

To support the advanced requirements of FO-PLP with its challenging features in the roadmap including small RDL line and spaces down to 2 µm and tall Cu pillars with increasing aspect ratios, the pre-treatment process prior to plating requires adequate wetting of the features to be plated. Wetting of standard features is achieved in a specially designed vertical tank under controllable flow conditions of chosen chemistries. These flow conditions are provided by direct jet flow from a flow distribution plate to ensure a uniform and controllable flow environment across the entire panel surface. Advanced wetting of more challenging features is achieved by use of a vertical vacuum

cell in which a controlled pressure drop leads to reduced partial pressure of the applied wetting medium. The result is a lowered surface tension allowing complete wetting of the feature.

The focus of development is of course in the plating cell system. Development topics center on the three principle pillars of plating such as fluid flow, current density distribution and chemical control.

Using hundreds of jets, evenly distributed across the anode segments, allows a novel approach of a direct fluid flow through the anode directly to the cathode surface.
This advanced flow technology, shown in figure 3, provides a highly uniform medium supply across the entire cathode surface and a high solution exchange at the boundary layer. Therefore high current densities and high plating speeds could be applied, while paddles or other hardware which can introduce undesired shielding or flow non-uniformities are not needed.

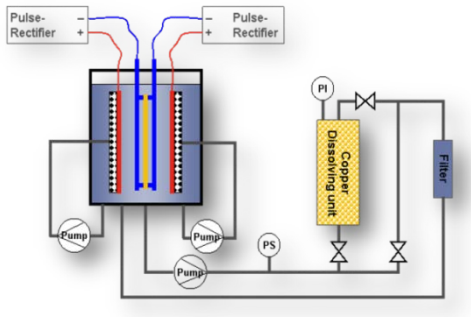

Figure 3. Plating cell fluid flow schematic of the MultiPlate® panel plating equipment

Further fluid flow optimization is achieved by physical agitation of the cathode which adds a very important process parameter. Localized flow phenomenon can be equalized by a predictable and repeatable controlled approach using freely programmable agitation profiles.

Applying a customized current density profile to large rectangular and square substrates is achieved using segmented anodes. The number of segments chosen and geometry of each segment is designed to optimize uniformity control for each substrate's geometry. Controlling the current to individual anode segments is a major control knob for optimizing plating uniformity across large panel substrates, especially when coupled with a pulse reverse rectifier. The ability to apply complex pulse profiles enabled across multiple anode segments offers a significant degree of process control.

Chemical control is the third pillar of plating. Absolute control of chemistry is accomplished by way of a specially developed version of Fe^{2+}/Fe^{3+} redox system for Cu replenishment & control. The system consists of a "Cu Tower" of pellets through which electrolyte passes for Cu replenishment. The plating system does not use soluble anodes; thereby the "Cu Tower", located outside of plating area, is the source of Cu ions. A PID controller working with input data from an inline spectrometer analyzing Cu and Fe concentrations controls both the Cu and Fe content within a defined specification by controlling the amount of flow through the "Cu Tower". Electrolyte additive concentrations are monitored and dosed via slipstreams taken from the main fluid flow path within a defined sample schedule. The slipstream is connected to a fully automated analytical system and to a manual sample port. Dosing of additives is also accomplished via the slipstream. The combined use of the Fe^{2+}/Fe^{3+} redox system using inert anodes provides both a reduced maintenance system and high plating performance stability.

In this new emerging market for FO-PLP, an easily overlooked and under-addressed topic is substrate handling. As each player in FO-PLP has their own experiences and manufacturing supply chains, each has their own approach to substrate delivery and environmental conditions.

While some may utilize open cassettes capable of 15 substrates, others have a more semiconductor fab approach with an enclosed FOUP-like substrate carrier. There is no standard approach and thus substrate handling is proving to be a critical technology to be seriously considered. The currently used approaches utilizing both Bernoulli end effectors for a nearly "touchless" handling and vacuum end effectors might not be sufficient anymore for the upcoming big and heavy panels.

Finally latest developments in package designs with through-mold-via interconnections or double-sided RDL layers require simultaneous plating on both sides of the substrate. This technique is fairly common in PCB manufacturing but a new approach in the BEOL industry. Consequently, substrates need to be implemented in a frame or substrate holder to allow plating from both sides.

C. Challenges for Equipment Development

Managing the high cost of development and meeting current process road-maps with an acceptable CoO prove to be the two main challenges for equipment development. Without market consensus or standardized panel size adoptions among the group of early players, customized hardware must be developed at high investment levels for each panel size. Considering the development efforts within 200 mm and 300 mm wafers, the extrapolation of those

investments to the multiple spreads in format area increases among the many panel formats is considerable. The format comparison of wafer and panel illustrates just a sample of the 10+ formats currently in development.

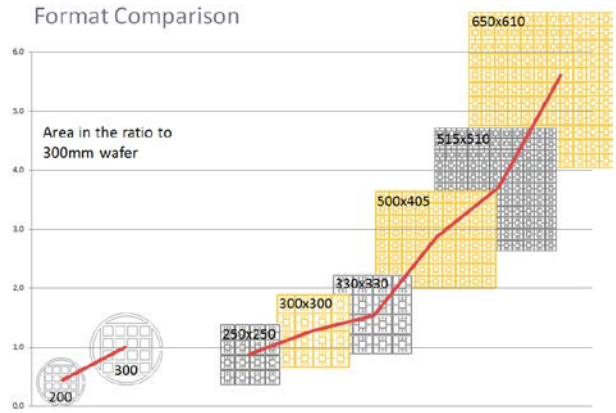

Figure 4. Area comparison of different wafer and panel formats

To illustrate the extent of the equipment set with the plating module, each format size can require a specific equipment package consisting of panel holder, anode set, tank, flow distribution box, rectifier, high amperage electrical setup. Each piece within the equipment package must be developed to achieve the process roadmap targets at lowest possible cost. Achieving equipment solutions which meet the CoO target which justifies the move to larger panel formats will lead to early adoption of the panel format. The current target for the Panel Plating Equipment CoO advantage over wafer which many players are seeking is greater than 40%.

IV. RESULTS

To achieve the yield and functionality of the packages produced by fan out panel level packaging it is necessary to have a WIPD below ±10 %. To reach this challenging goal a 3 step optimization is applied (please refer to figure 5).

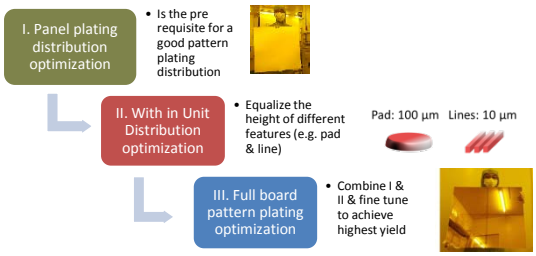

Figure 5. Optimization steps in RDL plating.

In the next diagram the process flow for the optimization of panel plating distribution is shown (step I.). As it is still unclear which panel size will be the direction for PLP, the optimizations of two panel formats are depicted.

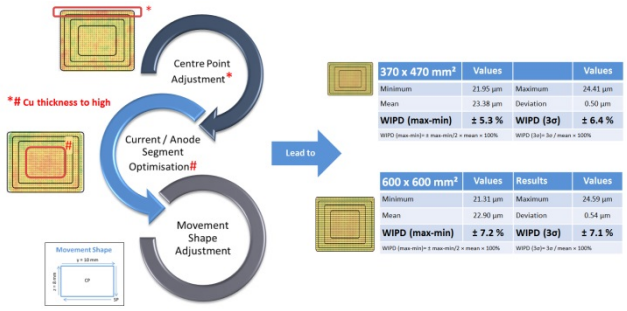

Figure 6. WIPD optimization sequence.

The first step is to adjust centre points of the substrate to the actual plating anodes. Secondly, current adjustments of the segmented anodes are needed to fine tune the overall plating distribution. Finally the definition of the substrate agitation profile is used to optimize the plating uniformity. By this procedure it was possible to reduce the WIPD for formats up to 600 × 600 mm² close to ±7 % and further optimization is ongoing. These measurements were done by automated 4 point probe resistivity measurements (e.g. over 3,000 measurement points for 600 × 600 mm² panels).

The second step of the optimization is the parameter tuning for best With-In-Unit-Distribution, which means to equalize the plating height of different features in the same unit. Of course very important for the final result is the RDL pattern itself. This pattern is of major importance for the With-In-Unit-Distribution (WIUD). In most of the cases the WIUD can hardly be changed, the main knobs for this optimization are the chemical parameters and the current density. Here we would like to show the influence of Reverse Pulse Plating (RPP) on the WIUD on the features shown in figure 7 (15 µm line & 150 µm pad).

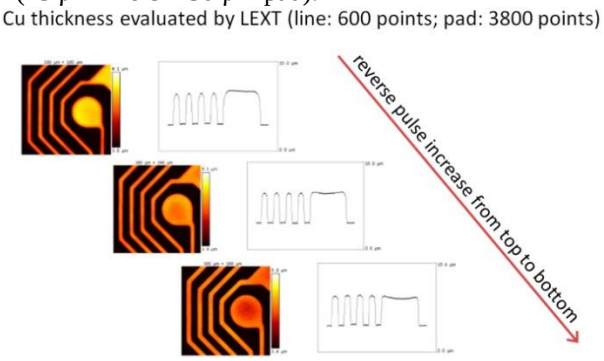

Figure 7. Optimization of WIUD by RPP.

In figure 7 one can see that under DC like conditions the pad has higher plating thickness than the traces. By increasing the reverse current the thicknesses can be equalized and even changed to the opposite. This becomes

even clearer, when the pad height is normalized to 100 % and the line height is shown in relation to that, which is shown in figure 8 in dependence of two different pump pressures.

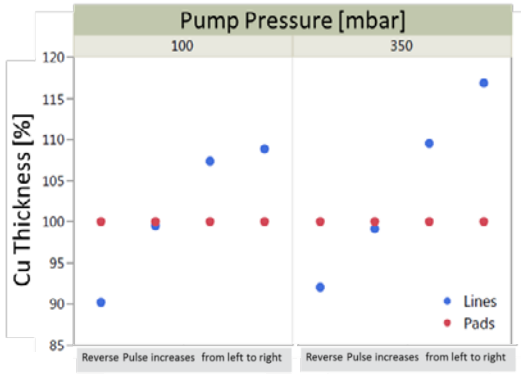

Figure 8. Optimization of WIUD by RPP.

The last step is the full panel RDL optimization, which involves several unique MultiPlate® features (e.g. changing the agitation by combining different movements; centre point adjustments & flow and pulse parameter adjustments). The RDL plating result for 600 × 600 mm² are given in figure 9.

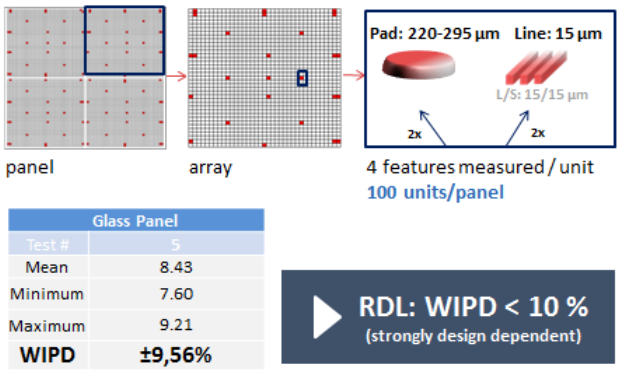

Figure 9. Optimization of WIPD by RPP.

As mentioned above, the RDL pattern design is very important for the final distribution result, but for various panel formats (250 × 250 mm²; 370 × 470 mm²; 510 × 415 mm²; 510 × 515 mm² & 600 × 600 mm²) we were able to achieve that the WIPD was better than ±10%. The measurement has been done according to customer specifications.

V. Conclusion

Upscaling the substrate area for Cu plating from round wafer substrates to square panel based processing is not as easy as it seems as two worlds collide: on the one hand there is the cost intensive wafer packaging world with its technical requirements and standards on the other hand the PCB and LCD world with its existing, cost effective process and equipment solutions. To cut costs down and to merge the two worlds, solutions have to be found for photolithography, substrate and Cu deposition. RDL creation is seen as main cost influencing factor and offering the highest chances for cost reduction. First solutions are now being installed in pilot lines for panel based Fan-Out technology.

The demonstrated new developments in plating materials and dedicated panel plating equipment clearly show feasibility with already available solutions existing today. Progress was made in development of optimised fluid flow, current density distribution and chemical control. In combination with our chemical plating process, we can meet the challenges that exist for RDL features on substrates with sizes of up to 600 × 600 mm² such as uniformity distribution of close to ±7 % as well as for and high speed plating of Tall Pillar structures of up to 200 µm height. The introduced system also allows the usage of special reverse pulse parameters which can tweak the WIUD on features like lines and pads.

Working together with many cooperation partners we see the main challenge in standardization of panel formats. A wide range of different substrate formats are currently under investigation, i.e. 300×300mm, 370×470mm, 508×508mm, 510×515mm , 600×600mm or even larger.
A consensus and final standardization of substrate size and format will be required to finally fulfil the cost improvements promise of Fan-Out Panel Level Packaging.

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