Filling of Microvias and Through Holes by Electrolytic Copper Plating – Current Status and Future Outlook

Mustafa Özkök, Sven Lamprecht, Akif Özkök, Dolly Akingbohungbe, Moody Dreiza
Atotech Deutschland GmbH
Berlin, Germany

Alex Stepinski
GreenSource Fabrication LLC
Charlestown, NH, USA

Abstract
The electronics industry is further progressing in terms of smaller, faster, smarter and more efficient electronic devices. This continuous evolving environment caused the development on various electrolytic copper processes for different applications over the past several decades.

There are 4 main drivers which forced the chemical supply industry to introduce new electrolytic copper processes with the new feature of "filling" capability over the years. The 1st driver is the continuous miniaturization of electronics. The first blind microvias were introduced with HDI technology in the late 1980s and early 1990s. In 1996, the IC Substrate market started to fill the micro vias. "Plugging" technologies were introduced in order to stack the micro vias to save space or to create "via in Pad" structures. This "plugging" technology with conductive paste was very expensive because of the additional process steps required.

Today copper filled microvias are the standard for almost all HDI PCB manufacturers. The 2nd driver is the thermal management on a substrate. Solutions were needed to integrate features with high thermal conductivity to manage the heat transfer on the substrates from one side to the other in order to minimize hot spots on the electronic devices over a lifetime. The higher the chip performance is, the more it tends to generate local heat-spots resulting in an early loss of the electronics in the field. The reason for this is the degeneration of various materials at these local hot spots.

Meanwhile the complete copper filled through holes was realized in 2006, by bridge plating or X -plating technology. Nowadays, completely copper filled through hole structures are at the leading edge of technology for thermal via structures because copper has almost the best thermal conductivity and it has to be plated nonetheless. The 3rd driver is the signal frequency. Electronic signals in an electronic package or inside of a PCB are increasing over time and continue to do so. Stacked microvias and fan-out vias are becoming more and more of a disadvantage for the transmission of high frequency signals, due to the fact of creating resistances at high frequencies. Therefore the push of high frequency applications further increased the demand for technologies like copper filled through holes.

The 4th driver especially for through hole filling, is the quality-yield aspect. The alternatives for electroplated copper filled through holes, requires many additional process steps, or new materials such as plugging pastes. Each of these additional process steps or materials introduces a variety of risks and manufacturing problems resulting in lower yield. Therefore the "one step" solution to fill through holes with copper is the preferred solution, without introducing new materials into the PCB. This paper describes the reasons for development and a roadmap of dimensions for copper filled through holes, microvias and other copper plated structures on PCBs. The paper will contain aspect ratios, dimensions and results of plated through holes used today in high volume manufacturing for

microvia and through hole filling with electroplated copper. Furthermore, it will also show feasibility studies of new electroplated structures for future applications such as copper pillar plating on IC-substrates.

Introduction

The electronics industry is progressing to smaller, faster, smarter and more efficient electronic devices. This continuous evolving environment boosted the development of various electrolytic copper processes for different applications over the past several decades. There are 4 main drivers which forced the chemical supply industry to introduce new electrolytic copper processes with the new feature of “filling” capability over the years.

The first driver is the continuous miniaturization of electronics. The first blind microvias were introduced in the late 1980s and early 1990s. In 1996, the market started to fill the micro vias. “Plugging” technologies were introduced in order to stack the micro vias to save space or to create “via in pad” structures. This “plugging” technology with conductive paste is very expensive because of the additional process steps required. In addition, this technology faced several disadvantages like “blow out”, “outgasing”, “smear”, and other quality concerns. In order to achieve this kind of miniaturization benefits, the industry was leaning towards the completely copper filled blind microvia rather than a plugged microvia as the leading edge solution. Today copper filled microvias are the standard for almost all HDI PCB manufacturers.

The second driver is the thermal management on a substrate. Here it is worthwhile to review a statement in this area: “As the power and packing density of electronic components increase, the amount of waste heat generated in a small space also rises greatly. This results in dangerously high temperatures and thus increases the failure risk of electronic devices. Today, 55 percent of electronic component failures are caused by increased temperatures alone.” [1]

Solutions were needed to integrate features with high thermal conductivity to manage the heat transfer on the substrates from one side to the other, in order to minimize hot spots on the electronic devices over a lifetime. Higher-performing chips tend to generate local hot-spots resulting in material degradation and premature field failure. Integration of thermal vias in high performance electronics can minimize the occurrence of hot spots and their utilization in the industry has therefore become more widespread. In the beginning, thermal vias were nothing more than standard conformal vias but the thermal conductivity was not good enough. Following that, plugging pastes were introduced in order to enhance the thermal conductivity of a standard through hole. But in this case, similar disadvantages of plugging appeared. Meanwhile complete copper filled through hole was realized in 2006, first by the bridge-plating or the X-plating technology. Nowadays, completely copper filled through hole structures are at the leading edge of technology for thermal via structures because copper has one of the best thermal conductivities and it has to be plated nonetheless.

The third driver is the signal frequency. Electronic signal frequencies in an electronic package or inside of a PCB are increasing over time and continue to do so. Fan-out vias are becoming more and more of a disadvantage for the transmission of high frequency signals, due to the fact of creating resistances at high frequencies. Therefore the push of high frequency applications further increased the demand for technologies like copper filled through holes. The 5G infrastructure in this moment is using the copper filled through hole technology in the field of smartphones already.

The fourth driver especially for through hole filling, is the quality-yield aspect. The alternatives for electroplated copper filled through holes, requires many additional process steps, or new materials such as plugging pastes. Each of these additional process steps or materials introduces a variety of risks and manufacturing problems resulting in lower yield. Therefore the “one step” solution to fill through holes with copper is the preferred solution, without introducing new materials into the PCB.

This paper describes the reasons for development and a roadmap of dimensions for copper filled through holes, microvias and shows aspects of other copper plated structures on PCBs. The paper will discuss aspect ratios, dimensions and results of plated through holes used today in high volume manufacturing for microvia and through hole filling with electroplated copper. Furthermore, it will also show feasibility studies of new electroplated structures for future applications such as copper pillar plating on IC-substrates.

Microvia Filling with Copper

The filling of microvias with copper was established as a “standard” in the PCB HDI production more than 20 years ago. There was the introduction of superviafilling technology with very low plated copper thickness on the surface (Figure 1).

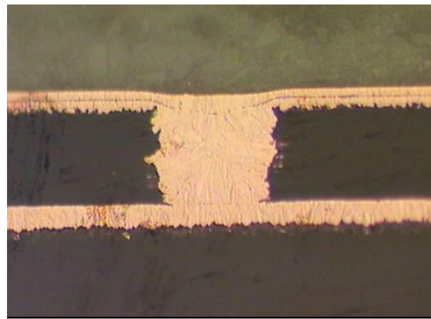

Figure 1 –Supervia fillingtechnology

Meanwhile the copper filling of microvias replaced many other filling technologies like plugging and capping realized by paste printing and plating over with copper (Figure 3). Both technologies Plugging/capping and copper filled microvias are enabling the so called “Via-in-Pad” structure which does have the advantage for PCB designers. The advantages of the “Via-in-Pad” designs are useful for high speed designs.

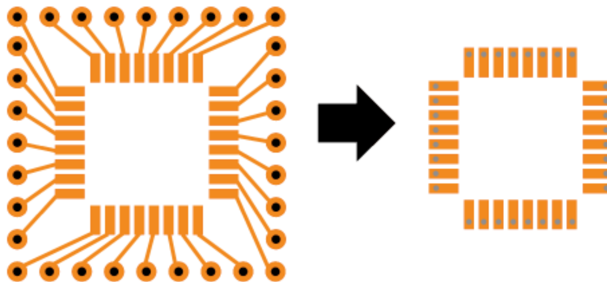

Figure 2 - TQFP footprint with vias and via-in-pads

Additionally copper filled microvias have significant advantages over plugging technology. The advantages are that the material inside the microvia is copper, while other materials have the potential to outgas or introduce different CTE values. Furthermore, voids in copper-filled µvias are far less common than with poor controlled conventional plugging methods.

Figure 3 - Plugged and capped microvia [2]

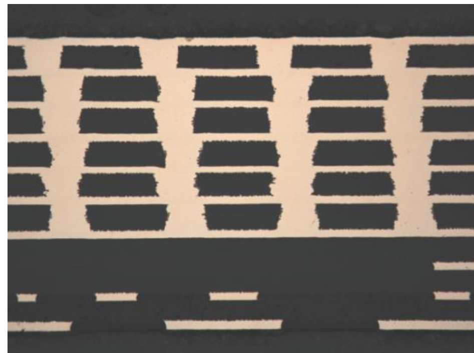

Figure 4 – Any layer technology stacked and filled with electrolytic plated copper

The development and introduction of copper filled microvias opened the door to introduce the so called any layer HDI technology shown in Figure 4. The any layer HDI technology enables copper filled through holes by stacking the copper filled microvias. This kind of feature enables HDI board designers the flexibility to create complex signal paths through the PCB by just using copper filled microvias.

Today almost all critical dimensions of microvias may be filled inclusion free with copper. Table 1 does show the microvia dimensions which can be filled today in horizontal and vertical plating equipment. The numbers inside the cells reflect the aspect ratios. The table represents the capability of various electrolytic copper formulations on the market. Each electrolytic copper recipe has its own characteristic abilities with regards to aspect ratio.

Table 1 - Copper filled Microvias: Dimensions which can be filled today

BMV Diameter [µm] \ BMV depth [µm]	10	15	20	25	30	35	40	45	50	55	60	65	70	75	80	85	90	95	100	105	110	115	120	125	130	135	140	145	150
200	0,1	0,1	0,1	0,1	0,2	0,2	0,2	0,2	0,3	0,3	0,3	0,3	0,4	0,4	0,4	0,4	0,5	0,5	0,5	0,5	0,6	0,6	0,6	0,6	0,7	0,7	0,7	0,7	0,8
190	0,1	0,1	0,1	0,1	0,2	0,2	0,2	0,2	0,3	0,3	0,3	0,3	0,4	0,4	0,4	0,4	0,5	0,5	0,5	0,6	0,6	0,6	0,6	0,7	0,7	0,7	0,7	0,8	0,8
180	0,1	0,1	0,1	0,1	0,2	0,2	0,2	0,3	0,3	0,3	0,3	0,4	0,4	0,4	0,4	0,5	0,5	0,5	0,6	0,6	0,6	0,6	0,7	0,7	0,7	0,8	0,8	0,8	0,8
170	0,1	0,1	0,1	0,1	0,2	0,2	0,2	0,3	0,3	0,3	0,4	0,4	0,4	0,4	0,5	0,5	0,5	0,6	0,6	0,6	0,6	0,7	0,7	0,7	0,8	0,8	0,8	0,9	0,9
160	0,1	0,1	0,1	0,2	0,2	0,2	0,3	0,3	0,3	0,3	0,4	0,4	0,4	0,5	0,5	0,5	0,6	0,6	0,6	0,7	0,7	0,7	0,8	0,8	0,8	0,8	0,9	0,9	0,9
150	0,1	0,1	0,1	0,2	0,2	0,2	0,3	0,3	0,3	0,4	0,4	0,4	0,5	0,5	0,5	0,6	0,6	0,6	0,7	0,7	0,7	0,8	0,8	0,8	0,9	0,9	0,9	1,0	1,0
140	0,1	0,1	0,1	0,2	0,2	0,3	0,3	0,3	0,4	0,4	0,4	0,5	0,5	0,5	0,6	0,6	0,6	0,7	0,7	0,8	0,8	0,8	0,9	0,9	0,9	1,0	1,0	1,0	1,1
130	0,1	0,1	0,2	0,2	0,2	0,3	0,3	0,3	0,4	0,4	0,5	0,5	0,5	0,6	0,6	0,7	0,7	0,7	0,8	0,8	0,8	0,9	0,9	1,0	1,0	1,0	1,1	1,1	1,2
120	0,1	0,1	0,2	0,2	0,3	0,3	0,3	0,4	0,4	0,5	0,5	0,5	0,6	0,6	0,7	0,7	0,8	0,8	0,8	0,9	0,9	1,0	1,0	1,0	1,1	1,1	1,2	1,2	1,3
110	0,1	0,1	0,2	0,2	0,3	0,3	0,4	0,4	0,5	0,5	0,5	0,6	0,6	0,7	0,7	0,8	0,8	0,9	0,9	1,0	1,0	1,0	1,1	1,1	1,2	1,2	1,3	1,3	1,4
100	0,1	0,2	0,2	0,3	0,3	0,4	0,4	0,5	0,5	0,6	0,6	0,7	0,7	0,8	0,8	0,9	0,9	1,0	1,0	1,1	1,1	1,2	1,2	1,3	1,3	1,4	1,4	1,5	1,5
90	0,1	0,2	0,2	0,3	0,3	0,4	0,4	0,5	0,6	0,6	0,7	0,7	0,8	0,8	0,9	0,9	1,0	1,1	1,1	1,2	1,2	1,3	1,3	1,4	1,4	1,5	1,6	1,6	1,7
80	0,1	0,2	0,3	0,3	0,4	0,4	0,5	0,6	0,6	0,7	0,8	0,8	0,9	0,9	1,0	1,1	1,1	1,2	1,3	1,3	1,4	1,4	1,5	1,6	1,6	1,7	1,8	1,8	1,9
70	0,1	0,2	0,3	0,4	0,4	0,5	0,6	0,6	0,7	0,8	0,9	0,9	1,0	1,1	1,1	1,2	1,3	1,4	1,4	1,5	1,6	1,6	1,7	1,8	1,9	1,9	2,0	2,1	2,1
60	0,2	0,3	0,3	0,4	0,5	0,6	0,7	0,8	0,8	0,9	1,0	1,1	1,2	1,3	1,3	1,4	1,5	1,6	1,7	1,8	1,8	1,9	2,0	2,1	2,2	2,3	2,3	2,4	2,5
50	0,2	0,3	0,4	0,5	0,6	0,7	0,8	0,9	1,0	1,1	1,2	1,3	1,4	1,5	1,6	1,7	1,8	1,9	2,0	2,1	2,2	2,3	2,4	2,5	2,6	2,7	2,8	2,9	3,0
40	0,3	0,4	0,5	0,6	0,8	0,9	1,0	1,1	1,3	1,4	1,5	1,6	1,8	1,9	2,0	2,1	2,3	2,4	2,5	2,6	2,8	2,9	3,0	3,1	3,3	3,4	3,5	3,6	3,8
30	0,3	0,5	0,7	0,8	1,0	1,2	1,3	1,5	1,7	1,8	2,0	2,2	2,3	2,5	2,7	2,8	3,0	3,2	3,3	3,5	3,7	3,8	4,0	4,2	4,3	4,5	4,7	4,8	5,0
20	0,5	0,8	1,0	1,3	1,5	1,8	2,0	2,3	2,5	2,8	3,0	3,3	3,5	3,8	4,0	4,3	4,5	4,8	5,0	5,3	5,5	5,8	6,0	6,3	6,5	6,8	7,0	7,3	7,5
10	1,0	1,5	2,0	2,5	3,0	3,5	4,0	4,5	5,0	5,5	6,0	6,5	7,0	7,5	8,0	8,5	9,0	9,5	10,0	10,5	11,0	11,5	12,0	12,5	13,0	13,5	14,0	14,5	15,0

Colour	AR	AR	Description
(green)	AR: 0,30 -1,00		Non critical aspect ratio
(bright green)	AR: 0,20 -0,29	AR: 1,01 -1,30	Feasible aspect ratio
(light green)	AR: 0,10 -0,19	AR: 1,31 -1,50	leading edge aspect ratio
(white)	AR: < 0,3	AR: >1,5	limited data

The numbers inside the cells reflects the aspect ratio (AR)

Table 2 - Copper filled Through Holes: Dimensions which can be filled today

Hole Diameter [mm]																				
0,50	0,1	0,2	0,3	0,4	0,5	0,6	0,7	0,8	0,9	1,0	1,1	1,2	1,3	1,4	1,5	1,6	1,7	1,8	1,9	2,0
0,45	0,1	0,2	0,3	0,4	0,6	0,7	0,8	0,9	1,0	1,1	1,2	1,3	1,4	1,6	1,7	1,8	1,9	2,0	2,1	2,2
0,40	0,1	0,3	0,4	0,5	0,6	0,8	0,9	1,0	1,1	1,3	1,4	1,5	1,6	1,8	1,9	2,0	2,1	2,3	2,4	2,5
0,35	0,1	0,3	0,4	0,6	0,7	0,9	1,0	1,1	1,3	1,4	1,6	1,7	1,9	2,0	2,1	2,3	2,4	2,6	2,7	2,9
0,30	0,2	0,3	0,5	0,7	0,8	1,0	1,2	1,3	1,5	1,7	1,8	2,0	2,2	2,3	2,5	2,7	2,8	3,0	3,2	3,3
0,25	0,2	0,4	0,6	0,8	1,0	1,2	1,4	1,6	1,8	2,0	2,2	2,4	2,6	2,8	3,0	3,2	3,4	3,6	3,8	4,0
0,20	0,3	0,5	0,8	1,0	1,3	1,5	1,8	2,0	2,3	2,5	2,8	3,0	3,3	3,5	3,8	4,0	4,3	4,5	4,8	5,0
0,15	0,3	0,7	1,0	1,3	1,7	2,0	2,3	2,7	3,0	3,3	3,7	4,0	4,3	4,7	5,0	5,3	5,7	6,0	6,3	6,7
0,10	0,5	1,0	1,5	2,0	2,5	3,0	3,5	4,0	4,5	5,0	5,5	6,0	6,5	7,0	7,5	8,0	8,5	9,0	9,5	10,0
0,05	1,0	2,0	3,0	4,0	5,0	6,0	7,0	8,0	9,0	10,0	11,0	12,0	13,0	14,0	15,0	16,0	17,0	18,0	19,0	20,0
	0,05	0,10	0,15	0,20	0,25	0,30	0,35	0,40	0,45	0,50	0,55	0,60	0,65	0,70	0,75	0,80	0,85	0,90	0,95	1,00
	Board Thickness [mm]																			

	AR: 0,50 -2,00		Non critical aspect ratio
	AR: 0,03 -0,49	AR: 2,01 -3,00	Feasible aspect ratio
	AR: 0,20 -0,29	AR: 3,01 -5,00	leading edge aspect ratio
	AR: < 0,5	AR: >5,0	limited data

The numbers inside the cells reflects the aspect ratio (AR)

The leading edge electrolytic formulation for microvia filling shown on figure 5 has the following characteristics:

- Plated with current density of up to 2,5 A
- Creates a ductility of 25%
- Tensile strength 35 kNm²
- Dimple less than 5µm; Plating time < 40 min
- 13 µm copper thickness on surface and at the same time filling a 100* 89µm microvia completely

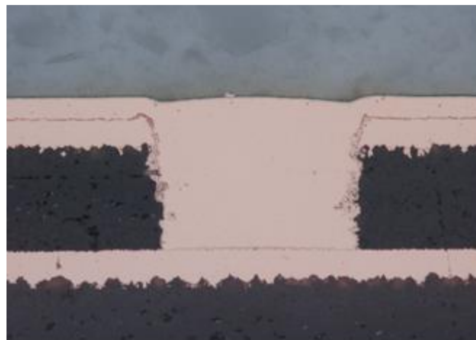

Figure 5 - Cu filled microvia cross section plated with a leading edge Cu Electrolyte

Through Hole Filling with Copper

The through hole filling of holes with copper in mass production has its roots in 2005. The introduction of X-plating or bridge plating was the beginning. The “bridging” technology was developed in order to fill a through hole completely with copper while avoiding inclusions. Such a completely filled through hole does have many advantages for the design of electronic PCBs such as thermal conductivity and signal integrity in high frequency boards.

A filled through hole may be realized in different ways. It may be plugged by a paste or filled by an electrolytic copper plating process.

For larger size of holes (diameter > 500µm) the plugging by a thermal conductive paste is the process mainly used. For smaller hole sizes (diameter < 500µm, and feasible aspect ratio (AR > 0.5 and <5.0) the copper filling using the bridge plating technology shows many advantages compared to paste plugging. First of all the bridge plating technology needs fewer manufacturing steps compared to paste plugging (refer to figure 6). This has a significant benefit for the production cost.

	plugging paste	copper plating
1	through via drilling	through via drilling
2	electroless copper seedlayer	electroless copper seedlayer
3	electrolytic copper conformal plating 25µm	electrolytic copper through via bridging & filling
4	plugging with paste	**dry film lamination**
5	paste curing	
6	mushroom grinding	
7	2nd electroless copper seedlayer	
8	2nd electrolytic copper plating cap plating 25- 55µm	
9	**dry film lamination**	

Figure 6 - plugging paste versus copper plating Through Hole Filling

The bridge plating technology offers a further advantage in terms of thermal conductivity compared to filling materials. Copper delivers one of the best thermal conductivity properties compared to lower thermal conductivity properties of any plugging paste on the market (Table 3).

Table 3 - Thermal conductivity of copper versus plugging paste

Layer Material	Thermal conductivity
Plugging Paste	~ 2-8 W/mK
Copper	~ 390 W/mK

This advantage enables PCB designers either to reduce the amount of thermal vias by about 70% while focusing thermal conducting and cooling efficiency at hotspots.

Table 4: Thermal Resistance of Copper versus Plugging Paste (Example: 1mm board thickness, 0,3mm diameter, 25µm copper barrel)

Layer Material		Total Thermal Resistance
25µm copper on side wall		*122 K/W*
Filled with	**Plugging paste**	*116 K/W*
	Copper	*37 K/W*

As illustrated in Figure 6 there are three reliability concerns with plugged vias that are negated by Copper plating. Whereas the void (1) and dimple (2) are process control related (lower risk) the blistering (3) is material and dimension related. The CTE mismatch of copper (16.5ppm) compared to plugging paste (30-50ppm) may result in a blister. These three phenomena on plugged vias have beeninvestigated [4].

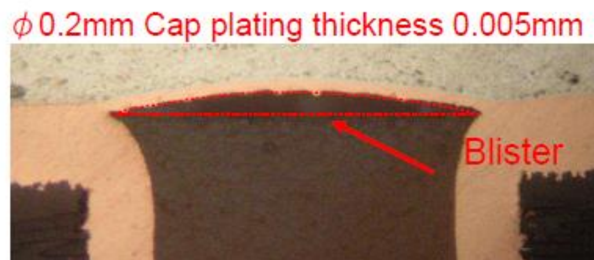

Figure 7 - plugging paste versus copper plating Through Hole Filling

Whereas plugging with paste may create all three phenomena, the blistering phenomenon is negated by using copper as the filling material. The formation void (1) also can be avoided fully using modern copper through hole filling processes (which operate void-free). This is achieved using, automated and sophisticated equipment controls during

the copper bridging and filling process. Furthermore the dimple (2) also is controlled below 5µm with the right settings on the copper process. These avoidance techniques are simply not possible when plugging a through hole via by a high viscosity plugging paste enabled using screen print methods.

The bridgeplating technology works as follows: During the first copper electroplating plating process a copper bridge is formed (Figure 8a). This bridge-plating is the key to fill the hole. After this step only two microvias on the top and the bottom are left which will be filled with copper by one or more subsequent microvia filling steps (Figure 8b-c).

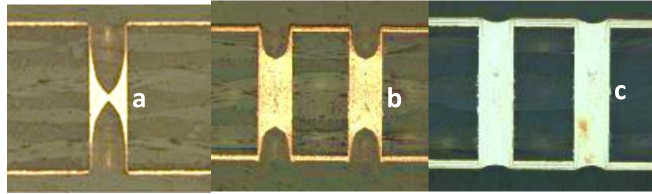

Figure 8 a-c - Generation of a copper filled Through Via

The copper bridge plating process works best with a horizontal copper plating process because the horizontal system offers key advantages in terms of fluid dynamics inside the hole. This promotes the generation of void free plating results, very low plated copper thickness on the surface, a much better copper uniformity and a higher throughput compared to vertical plating units.

The dimensions of through holes which are achievable with filled copper are illustrated in Table 4. This table is based on various commercially available copper electrolytes used in the latest generation horizontal plating equipment.

Current research and develop efforts regarding copper through hole filling cover the following topics:

a) faster processing time (cost driven)
b) to plate less copper on the surface (cost driven)
c) increase the uniformity (technology driven)
d) better filling performance, low dimple (technology driven)
e) keeping the void free level (quality driven)
f) selecting parameters to plate higher aspect ratios

Other New Electroplating Copper Technologies

As the technology of filling microvias and through holes is already established and in production, the electronic market requires newer features such as pillar plating realized on IC-Substrates or smaller RDL (Redistribution Layer) structures in order to enable Panel Level Packaging (PLP) on IC-Substrate Level. That development has already progressed quite far. A newer equipment approach with recently developed copper electrolytes does enable these technologies. The first copper plating equipment of this new generation offers the following:

1. Plating of a target Cu thickness of 6µm on a 600x600mm panel with a Cu thickness distribution of less than 5%.

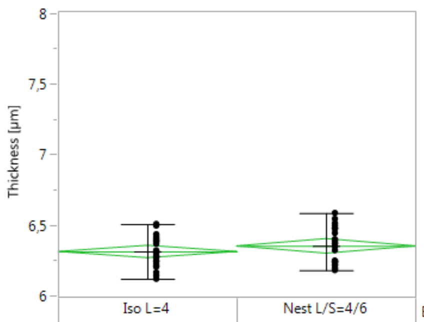

Figure 9 - Achieved Cu Thickness distribution on a 600x600mm Panel

2. Capable of filling microvias with a size of 15x10µm by having only 5µm plated thickness on the surface and a dimple less than 2µm.

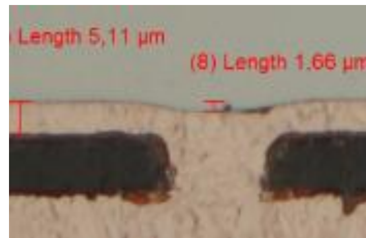

Figure 10 - Achieved Cu Thickness distribution on a 600x600mm Panel

Furthermore this new plating tool enables Panel Level Packaging Technology on IC Substrates. This allows the IC Substrates industry to compete with the Semiconductor Wafer Level Packaging Technologies and to plate new features such as copper pillars.

Summary
This paper presents the actual status of microvia filling and through hole filling realized by electrolytic copper plating processes. The dimensions of microvias and through holes which can be filled by electrolytic copper processes today are shown. Furthermore the copper filling technologies versus paste plugging were compared and the benefits of the copper filling technologies have been illustrated. The scope of future developments in terms of microvia filling and through hole filling have been addressed. Next Generation technology segments such as Panel Level Packaging (PLP) and also plating of copper pillars on IC Substrates, realized by a novel electrolytic copper plating processes were also considered.

References

[1] Website Fraunhofer IZM: https://www.ipm.fraunhofer.de
[2] Picture from www.we-online.com. Würthtechnologies.chapter micro via filling
[3] Picture from electronics.stackexchange.com. chapter via-in pad. technology
[4] S. Sano, *Current state and future trends ofPCBs in AVIO*. Netherlands: 5th EMPPS workshop, ch. 3.1, pp. 11-14.(2014)
[5] S.Lamprecht, *Plating a thermal runaway in PCBs -solid copper through via filling*. IPC workshop, ch. 3.1, pp. 11-14. (2018)